Interleaving Continuous Conduction Mode PFC Controller

Check for Samples: UCC28070

FEATURES

- Interleaved Average C 固有电流匹配的交错平均电流模式PWM
  Control with Inherent
- Advanced Current Syn 先进的电流整合检流，出色的转换效率
  Sensing for Superior E
- Highly-Linear Multiplie 内部量化电压前馈较正的高线性化乘法器
  Quantized Voltage Fee
  for Near-Unity PF
- Programmable Freque 频率（30k-300kHz）z)
- Programmable Maxim 最大占空比钳位
- Programmable Freque 可控的频率抖动速率和幅度或增强EMI抑制能力
  Magnitude for Enhanc
  - Magnitude: 3 kHz t 幅度：3k-30kHz
  - Rate: Up to 30 kHz 速率:可达30kHz
- External Clock Synch 外部时钟同步功能
- Enhanced Load and L 通过电压放大器输出速率校正提高负载和线性瞬态响应 se
  through Voltage Ampl
  Correction
- Programmable Peak C 可控的峰会电流限制
- Bias-Supply UVLO, Ov 偏置电源电压锁定，过压保护，开环检测
  Open-Loop Detection,
  Monitoring
- External PFC-Disable 外部PFC禁止端口
- Open-Circuit Protecti VSENSE和VINAC引脚开路保护
  VINAC pins
- Programmable Soft S 软启动
- 20-Lead TSSOP/SOIC 20脚TSSOP/SOIC封装

APPLICATIONS

- High-Efficiency Server and Desktop Power Supplies
- Telecom Rectifiers
- White Goods and Industrial Equipment

DESCRIPTION

The UCC28070 is an advanced power factor correction device that integrates two pulse-width modulators (PWMs) operating 180° out of phase. This interleaved PWM operation generates substantial reduction in the input and output ripple

UCC28070是一款先进的PFC芯片，有两路相位相关180的PWM输出。这种交错的PWM方式减小的输入输出的纹波电流，同时也使EMI滤波器设计变得简单并且成本降低。一个显著改进的乘法器为两路独立的电流放大器提供一个共享的电流参考，确保在两路PWM输出上匹配平均电流模式控制，同时保持稳定低失真的正弦输入线电流。

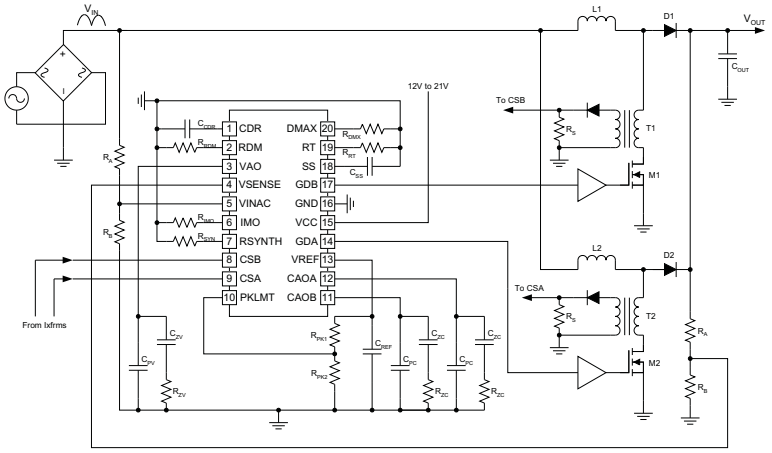
The UCC28070 contains multiple innovations including current synthesis and quantized voltage feed-forward to promote performance enhancements

UCC28070有多重创新，包括电流整合工量化电压前馈，提升了PF、效率、THD和瞬态响应性能。频率抖动，时钟同步和转换速率这些性能的增强进一步提升的潜在性能。

The UCC28070 also contains a variety of protection features including output over-voltage detection

UCC28070还包含了很多的保护功能，包括输出过压保护，可控的峰值电流限制，欠压锁定和开环保护。

Simplified Application Diagram



ORDERING INFORMATION

PART NUMBER	PACKAGE	PACKING
UCC28070PW	Plastic, 20-Pin TSSOP (PW)	70-Pc. Tube
UCC28070PWR	Plastic, 20-Pin TSSOP (PW)	2000-Pc. Tape and Reel
UCC28070DW	Plastic, 20-Pin SOIC (DW)	25-Pc. Tube
UCC28070DWR	Plastic, 20-Pin SOIC (DW)	2000-Pc. Tape and Reel

ABSOLUTE MAXIMUM RATINGS(1) (2) (3) (4)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	LIMIT	UNIT
Supply voltage: VCC	22	V
Supply current: I_{VCC}	20	mA
Voltage: GDA, GDB	−0.5 to VCC+0.3	V
Gate drive current – continuous: GDA, GDB	+/− 0.25	A
Gate drive current – pulsed: GDA, GDB	+/− 0.75	
Voltage: DMAX, RDM, RT, CDR, VINAC, VSENSE, SS, VAO, IMO, CSA, CSB, CAOA, CAOB, PKLMT, VREF	−0.5 to +7	V
Current: RT, DMAX, RDM, RSYNTH	−0.5	mA
Current: VREF, VAO, CAOA, CAOB, IMO	10	
Operating junction temperature, T_J	−40 to +125	°C
Storage temperature, T_{STG}	−65 to +150	
Lead temperature (10 seconds)	260	

(1) These are stress limits. Stress beyond these limits may cause permanent damage to the device. Functional operation of the device at these or any conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.
(2) All voltages are with respect to GND.
(3) All currents are positive into the terminal, negative out of the terminal.
(4) In normal use, terminals GDA and GDB are connected to an external gate driver and are internally limited in output current.

在正常使用情况下，GDA和GDB连接到外部门极驱动器，并由芯片内部限制了输出电流。

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	RATING	UNIT
Human Body Model (HBM)	2,000	V
Charged Device Model (CDM)	500	

DISSIPATION RATINGS

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	T_A = 25°C POWER RATING	T_A = 85°C POWER RATING
20-Pin TSSOP	125 °C/Watt (1) and (2)	800 mW (1)	320 mW (1)
20-Pin SOIC	95 °C/Watt (1) and (2)	1050 mW (1)	420 mW (1)

(1) Thermal resistance is a strong function of board construction and layout. Air flow reduces thermal resistance. This number is only a general guide.
(2) Thermal resistance calculated with a low-K methodology.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
VCC Input Voltage (from a low-impe	VCC输入电压（来自一个低阻抗电源）	V_{UVLO} + 1 V	21	V
VREF Load Current	VREF负载电流		2	mA
VINAC Input Voltage Range	VINAC输入电压范围	0	3	V
IMO Voltage Range	IMO电压范围	0	3.3	
PKLMT, CSA, & CSB Voltage Range	PKLMT,CSA,CSB电压范围	0	3.6	
RSYNTH Resistance (R_{SYN})	RSYNTH电阻	15	750	kΩ
RDM Resistance (R_{RDM})	RDM电阻	30	330	

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range −40°C < T_A < 125°C, T_J = T_A, VCC = 12 V, GND = 0 V, R_{RT} = 75 kΩ, R_{DMX} = 68.1 kΩ, R_{RDM} = R_{SYN} = 100 kΩ, C_{CDR} = 2.2 nF, C_{SS} = C_{VREF} = 0.1 µF, C_{VCC} = 1 µF, I_{VREF} = 0 mA (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Bias Supply						
VCC_{SHUNT}	VCC shunt voltage (1)	I_{VCC} = 10 mA	23	25	27	V
	VCC current, disabled	VSENSE = 0 V		7		mA
	VCC current, enabled	VSENSE = 3 V (switching)		9	12	
	VCC current, UVLO	VCC = 7 V			200	µA
		VCC = 9 V		4	6	mA
V_{UVLO}	UVLO turn-on threshold	Measured at VCC (rising)	9.8	10.2	10.6	V
	UVLO hysteresis	Measured at VCC (falling)		1		
	VREF enable threshold	Measured at VCC (rising)	7.5	8	8.5	
Linear Regulator						
	VREF voltage, no load	I_{VREF} = 0 mA	5.82	6	6.18	V
	VREF load rejection	Measured as the change in VREF, (I_{VREF} = 0 mA and −2 mA)	-12		12	mV
	VREF line rejection	Measured as the change in VREF, (VCC = 11V and 20 V, I_{VREF} = 0 µA)	-12		12	
PFC Enable						
V_{EN}	Enable threshold	Measured at VSENSE (rising)	0.65	0.75	0.85	V
	Enable hysteresis			0.15		
External PFC Disable						
	Disable threshold	Measured at SS (falling)	0.5	0.6		V
	Hysteresis	VSENSE > 0.85 V		0.15		
Oscillator						
	Output phase shift	Measured between GDA and GDB	179	180	181	Degree
V_{DMAX},V_{RT}, and V_{RDM}	Timing regulation voltages	Measured at DMAX, RT, & RDM	2.91	3	3.09	V
f_{PWM}	PWM switching frequency	R_{RT} = 75 kΩ, R_{DMX} = 68.1 kΩ, V_{RDM} = 0 V, V_{CDR} = 6 V	95	100	105	kHz
		R_{RT} = 24.9 kΩ, R_{DMX} = 22.6 kΩ, V_{RDM} = 0 V, V_{CDR} = 6 V	270	290	330	
D_{MAX}	Duty-cycle clamp	R_{RT} = 75 kΩ, R_{DMX} = 68.1 kΩ, V_{RDM} = 0 V, V_{CDR} = 6 V	92%	95%	98%	
	Minimum programmable off-time	R_{RT} = 24.9 kΩ, R_{DMX} = 22.6 kΩ, V_{RDM} = 0 V, V_{CDR} = 6 V	50	150	250	ns
f_{DM}	Frequency dithering magnitude change in f_{PWM}	R_{RDM} = 316 kΩ, R_{RT} = 75 kΩ	2	3	4	kHz
		R_{RDM} = 31.6 kΩ, R_{RT} = 24.9 kΩ	24	30	36	
f_{DR}	Frequency dithering rate rate of change in f_{PWM}	C_{CDR} = 2.2 nF, R_{RDM} = 100 kΩ		3		
		C_{CDR} = 0.3 nF, R_{RDM} = 100 kΩ		20		
I_{CDR}	Dither rate current	Measure at CDR (sink and source)		±10		µA
	Dither disable threshold	Measured at C_{CDR} (rising)		5	5.25	V

(1) Excessive VCC input voltage and/or current damages the device. This clamp will not protect the device from an unregulated supply. If an unregulated supply is used, a series-connected fixed positive voltage regulator such as a UA78L15A is recommended. See the Absolute Maximum Ratings section for the limits on VCC voltage and current.

过度的VCC输入会损坏芯片。这个钳压在紊乱的输入时将不会保护芯片。如果用了一个不稳定电源，建议串联一个稳压器（如UA78L15）使用。

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range −40°C < T_A < 125°C, T_J = T_A, VCC = 12 V, GND = 0 V, R_{RT} = 75 kΩ, R_{DMX} = 68.1 kΩ, R_{RDM} = R_{SYN} = 100 kΩ, C_{CDR} = 2.2 nF, C_{SS} = C_{VREF} = 0.1 µF, C_{VCC} = 1 µF, I_{VREF} = 0 mA (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Clock Synchronization						
V_{CDR}	SYNC enable threshold	Measured at CDR (rising)		5	5.25	V
	SYNC propagation delay	V_{CDR} = 6 V, Measured from RDM (rising) to GDx (rising)		50	100	ns
	SYNC threshold (Rising)	V_{CDR} = 6 V, Measured at RDM		1.2	1.5	V
	SYNC threshold (Falling)	V_{CDR} = 6 V, Measured at RDM	0.4	0.7		
	SYNC pulses	Positive pulse width	0.2			µs
		Maximum duty cycle (2)		50		%
Voltage Amplifier						
	VSENSE voltage	In regulation, T_A = 25°C	2.97	3	3.03	V
	VSENSE voltage	In regulation	2.94	3	3.06	
	VSENSE input bias current	In regulation		250	500	nA
	VAO high voltage	VSENSE = 2.9 V	4.8	5	5.2	V
	VAO low voltage	VSENSE = 3.1 V		0.05	0.50	
g_{MV}	VAO transconductance	2.8 V < VSENSE < 3.2 V, VAO = 3 V		70		µS
	VAO sink current, overdriven limit	VSENSE = 3.5 V, VAO = 3 V		30		µA
	VAO source current, overdriven	VSENSE = 2.5 V, VAO = 3 V, SS = 3 V		−30		
	VAO source current, overdriven limit + I_{SRC}	VSENSE = 2.5 V, VAO = 3 V		−130		
	Slew-rate correction threshold	Measured as VSENSE (falling) / VSENSE (regulation)	92	93	95	%
	Slew-rate correction hysteresis	Measured at VSENSE (rising)		3	9	mV
I_{SRC}	Slew-rate correction current	Measured at VAO, in addition to VAO source current.		−100		µA
	Slew-rate correction enable threshold	Measured at SS (rising)		4		V
	VAO discharge current	VSENSE = 0.5 V, VAO = 1 V		10		µA
Soft Start						
I_{SS}	SS source current	VSENSE = 0.9 V, SS = 1 V		−10		µA
	Adaptive source current	VSENSE = 2.0 V, SS = 1 V		−1.5	-2.5	mA
	Adaptive SS disable	Measured as VSENSE – SS	-30	0	30	mV
	SS sink current	VSENSE = 0.5 V, SS = 0.2 V	0.5	0.9		mA

(2) Due to the influence of the synchronization pulse width on the programmability of the maximum PWM switching duty cycle (D_{MAX}) it is recommended to minimize the synchronization signal's duty cycle.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range −40°C < T_A < 125°C, T_J = T_A, VCC = 12 V, GND = 0 V, R_{RT} = 75 kΩ, R_{DMX} = 68.1 kΩ, R_{RDM} = R_{SYN} = 100 kΩ, C_{CDR} = 2.2 nF, C_{SS} = C_{VREF} = 0.1 µF, C_{VCC} = 1 µF, I_{VREF} = 0 mA (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Over Voltage						
V_{OVP}	OVP threshold	Measured as VSENSE (rising) / VSENSE (regulation)	104	106	108	%
	OVP hysteresis	Measured at VSENSE (falling)		100		mV
	OVP propagation delay	Measured between VSENSE (rising) and GDx (falling)		0.2	0.3	µs
Zero-Power						
V_{ZPWR}	Zero-power detect threshold	Measured at VAO (falling)	0.65	0.75		V
	Zero-power hysteresis			0.15		
Multiplier						
k_{MULT}	Gain constant	VAO ≥ 1.5 V, T_A = 25°C	16	17	18	µA
		VAO = 1.2 V, T_A = 25°C	14.5	17.0	19.5	
		VAO ≥ 1.5 V	15	17	19	
		VAO = 1.2 V	13	17	21	
I_{IMO}	Output current: zero	VINAC = 0.9 V_{PK}, VAO = 0.8 V	-0.2	0	0.2	
		VINAC = 0 V, VAO = 5 V	-0.2	0	0.2	
Quantized Voltage Feed Forward						
V_{LVL1}	Level 1 threshold (3)	Measured at VINAC (rising)	0.6	0.7	0.8	V
V_{LVL2}	Level 2 threshold			1		
V_{LVL3}	Level 3 threshold			1.2		
V_{LVL4}	Level 4 threshold			1.4		
V_{LVL5}	Level 5 threshold			1.65		
V_{LVL6}	Level 6 threshold			1.95		
V_{LVL7}	Level 7 threshold			2.25		
V_{LVL8}	Level 8 threshold			2.6		
Current Amplifiers						
	CAOx high voltage		5.75	6		V
	CAOx low voltage				0.1	
g_{MC}	CAOx transconductance			100		µS
	CAOx sink current, overdriven			50		µA
	CAOx source current, overdriven			−50		
	Input common mode range		0		3.6	V
	Input offset Voltage	RSYNTH = 6 V, T_A = 25°C	-4	-8	-13	mV
		RSYNTH = 6 V	0	-8	-20	
	Input offset voltage		0	−8	−20	mV
	Phase mismatch	Measured as Phase A's input offset minus Phase B's input offset	-12	0	12	
	CAOx pull-down current	VSENSE = 0.5 V, CAOx = 0.2 V	0.5	0.9		mA

(3) The Level 1 threshold represents the "zero-crossing detection" threshold above which VINAC must rise to initiate a new input half-cycle, and below which VINAC must fall to terminate that half-cycle.

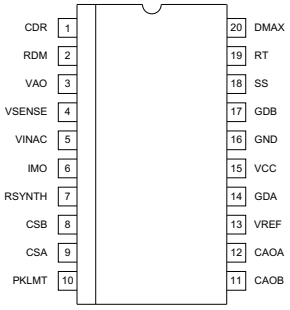
ELECTRICAL CHARACTERISTICS (continued)

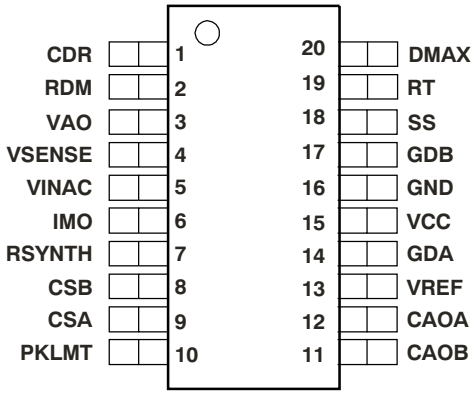
over operating free-air temperature range −40°C < T_A < 125°C, T_J = T_A, VCC = 12 V, GND = 0 V, R_{RT} = 75 kΩ, R_{DMX} = 68.1 kΩ, R_{RDM} = R_{SYN} = 100 kΩ, C_{CDR} = 2.2 nF, C_{SS} = C_{VREF} = 0.1 µF, C_{VCC} = 1 µF, I_{VREF} = 0 mA (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Synthesizer						
V_{RSYNTH}	Regulation voltage	VSENSE = 3 V, VINAC = 0 V	2.91	3	3.09	V
		VSENSE = 3 V, VINAC = 2.85 V	0.10	0.15	0.20	
	Synthesizer disable threshold	Measured at RSYNTH (rising)		5	5.25	
	VINAC input bias current			0.250	0.500	µA
Peak Current Limit						
	Peak current limit threshold	PKLMT = 3.30 V, measured at CSx (rising)	3.27	3.3	3.33	V
	Peak current limit propagation delay	Measured between CSx (rising) and GDx (falling) edges		60	100	ns
PWM Ramp						
V_{RMP}	PWM ramp amplitude		3.8	4.0	4.2	V
	PWM ramp offset voltage	T_A = 25°C, R_{RT} = 75 kΩ	0.65	0.7		
	PWM ramp offset temperature coefficient			−2		mV/ °C
Gate Drive						
	GDA, GDB output voltage, high, clamped	VCC = 20 V, C_{LOAD} = 1 nF	11.5	13	15	V
	GDA, GDB output voltage, High	C_{LOAD} = 1 nF	10	10.5		
	GDA, GDB output voltage, Low	C_{LOAD} = 1 nF		0.2	0.3	
	Rise time GDx	1 V to 9 V, C_{LOAD} = 1 nF		18	30	ns
	Fall time GDx	9 V to 1 V, C_{LOAD} = 1 nF		12	25	
	GDA, GDB output voltage, UVLO	VCC = 0 V, I_{GDA}, I_{GDB} = 2.5 mA		0.7	2	V
Thermal Shutdown						
	Thermal shutdown threshold			160		°C
	Thermal shutdown recovery			140		

DEVICE INFORMATION

SOIC-20 Top View, DW Package
TSSOP-20 Top View, PW Package





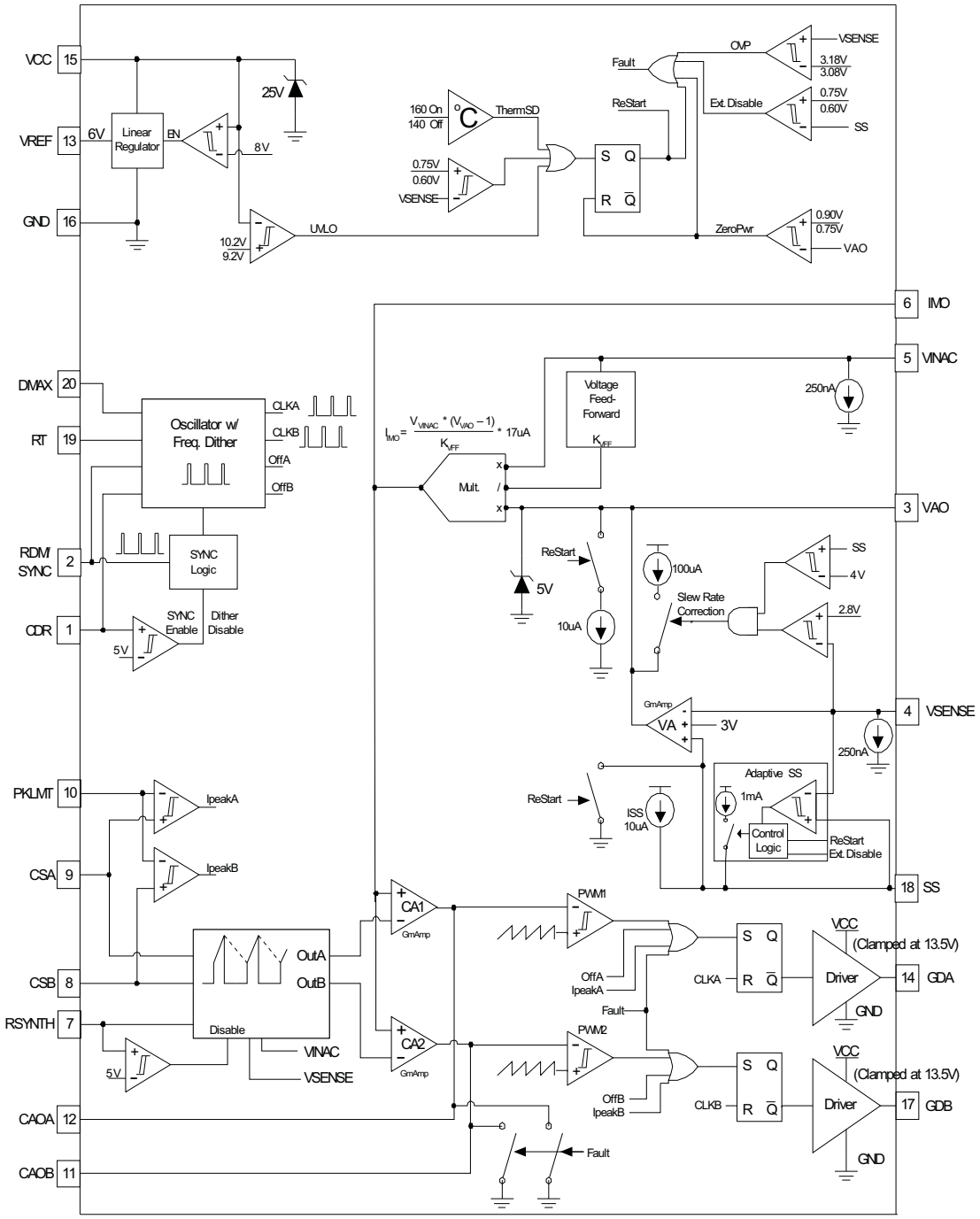
TERMINAL FUNCTIONS

NAME	PIN #	I/O	DESCRIPTION
CDR	1	I	抖动速率电容：频率抖动定时脚。接一个电容到GND来设置振荡器频率抖动速率。直接与VREF连接时禁止此功能。
RDM (SYNC)	2	I	抖动幅度电阻：频率抖动幅度和外部同步脚。接一个电阻到地来设置振荡器频率抖动幅度。当频率抖动功能禁止（CDR>5V）时，内部主时钟将在RDM脚的正边沿时同步。将RDM接地时禁用相关功能。 is not desired.
VAO	3	O	电压放大器输出。跨导电压放大器的输出。内部连接到乘法器输入和零功率比较器。电压调节环路补偿元件连接在这个脚和GND之间。
VSENSE	4	I	输出电压检测。内部除了电流整合差分放大器的正极输入外，连接到跨导电压误差放大器的反相输入端。也连接到了OVP，PFC使能，和转换速率比较器。通过一个电阻分压网络连接到PFC输出。
VINAC	5	I	采集AC线输入电压。内部连接到乘法器和电流整合误差放大器的负极端。在Vin,VINAC,和GND之间连接一个和PFC输出到VSENSE之间一样的电阻分压网络
IMO	6	O	乘法器电流输出。接一个电阻到地来设置乘法器增益。
RSYNTH	7	I	电流合成的下斜坡编程。接一个电阻到地来设置电流整合下斜坡的幅度。把RSYNTH接到VREF将禁止电流合成，并连接CSA和CSB直接连接到各自的放大器
CSB	8	I	相位B电流检测输入。在GDB导通时，CSB在内部通过电流整合阶段连接到B的电流放大器反相输入端
CSA	9	I	相位A电流检测输入。在GDA导通时，CSA在内部通过电流整合阶段连接到A的电流放大器反相输入端
PKLMT	10	I	峰值电流限制编程。连接一个电阻分压网络到VREF来设置逐周期峰值电流限制比较器的电压阈值。允许对要求的IIb校正

TERMINAL FUNCTIONS (continued)

NAME	PIN #	I/O	DESCRIPTION
CAOB	11	O	**Phase B Current Amplifier Output**. Output of phase B's transconductance current amplifier. Internally connected to the inverting input of phase B's PWM comparator for trailing-edge modulation. Connect the current regulation loop compensation components between this pin and GND. B电流放大器输出。B的跨导电流放大器的输出。内部连接到B的PWM比较器的反相输入作后缘调制。此脚到GND这间连接电流调节环路补偿元件。
CAOA	12	O	Internally connected to the inverting input of phase A's PWM comparator for trailing-edge modulation. Connect the current regulation loop compensation components between this pin and GND.
VREF	13	O	6V基准电压和内部偏置电压。接一个0.1uF电容到地，电容尽量靠近此引脚和地。
GDA	14	O	A的门极驱动。这个限电流的输出端将会连接到一个独立的适合驱动相位A的开关器件的门极驱动器件。输出电压被钳位在额定的13.5V
VCC	15	I	芯片电压输入。接一个0.1uF电容到地，电容尽量靠近此引脚和地。
GND	16	I/O	芯片接地引脚。所有补偿元件和设置用的电阻电容都要接到此脚。为隔离大电流噪声，要用独立的直线连接此脚与系统地。
GDB	17	O	**Phase B's Gate Drive**. This limited-current output is intended to connect to a separate gate-drivedevice suitable for driving the Phase B switching component(s). The output voltage is typically clamped to 13.5 V.
SS	18	I	软启动和外部故障接口。接一个电容到地，能过内部10uA恒流源对此电容充电来设置软启动速率。VSENSE的调节参考电压被钳位在Vss，直到Vss超过3V后才被释放。在从某些故障情况下恢复时，SS在没有与VSENSE相等之前SS存在一个1mA的电流源。所SS脚拉低到0.6V以下将禁止GDA和GDB输出 outputs.
RT	19	I	定时电阻。振荡器频率设置引脚。接一个电阻到地来设置内部振荡器的运行频率。
DMAX	20	I	最大占空比电阻。设置电大PWM占空比的引脚。接一个电阻到地，以Rdmx:Rrt的比值来设置PWM的最大占空比

Functional Block Diagram



TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs TEMPERATURE

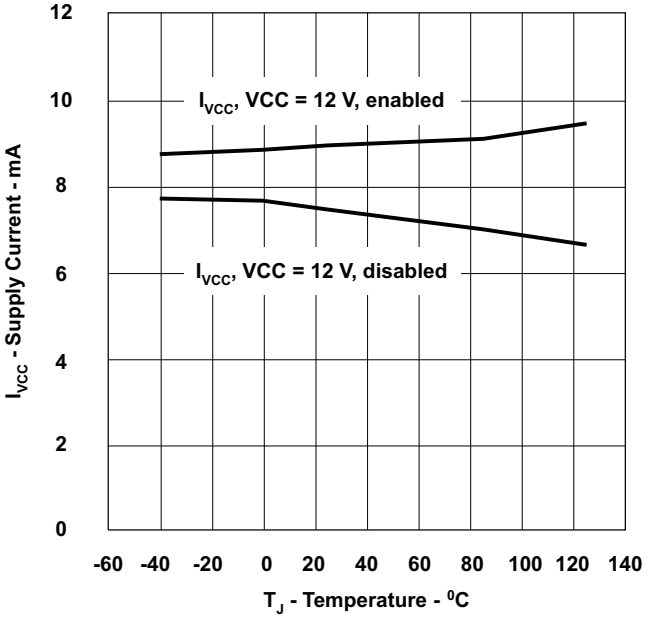


Figure 1.

REFERENCE VOLTAGE vs TEMPERATURE

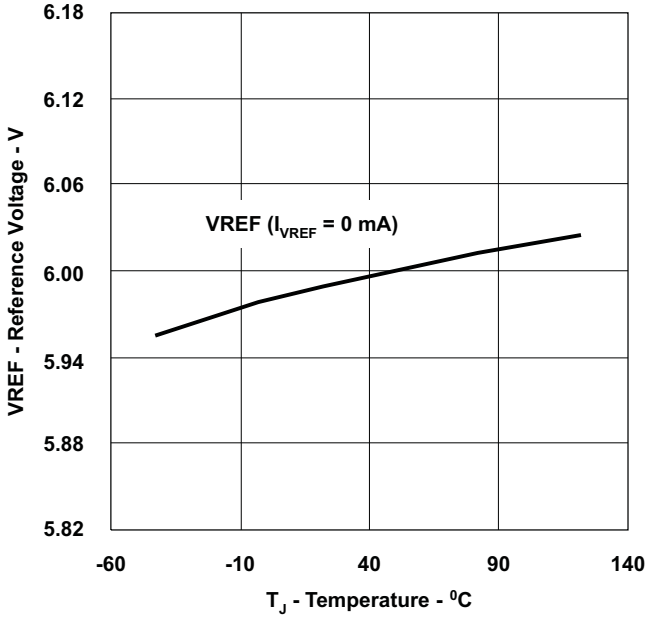


Figure 2.

VSENSE REGULATION vs TEMPERATURE

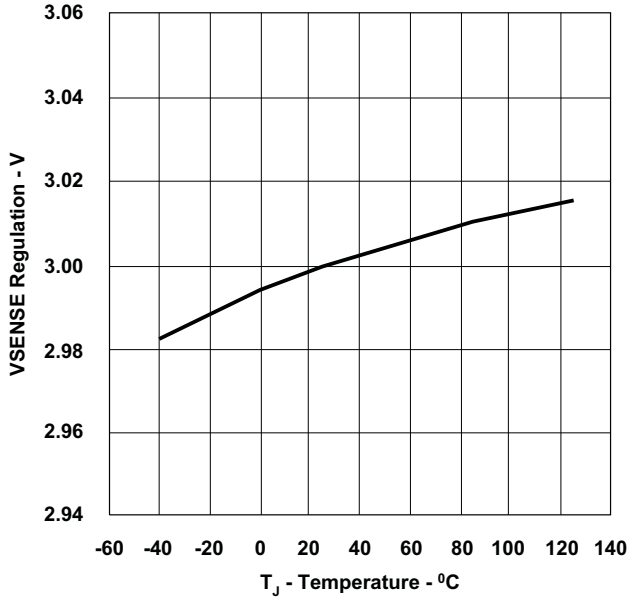


Figure 3.

I_{VSENSE} BIAS CURRENT vs TEMPERATURE

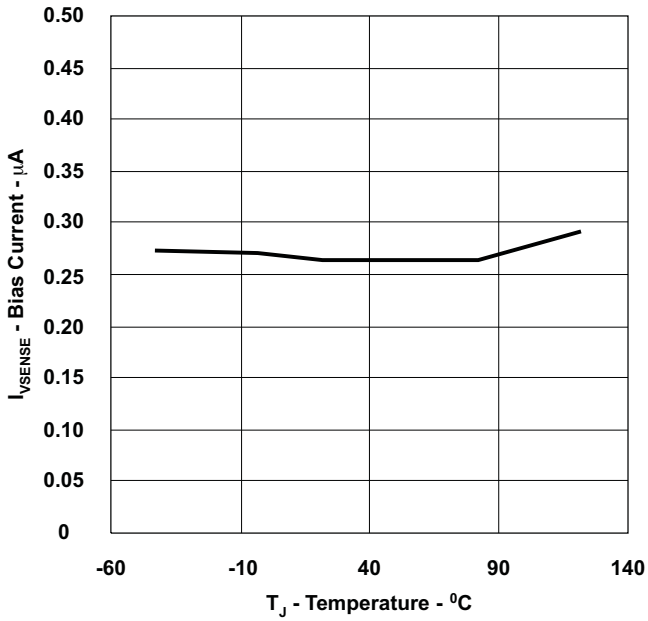


Figure 4.

TYPICAL CHARACTERISTICS (continued)

MULTIPLIER OUTPUT CURRENT vs VOLTAGE AMPLIFIER OUTPUT

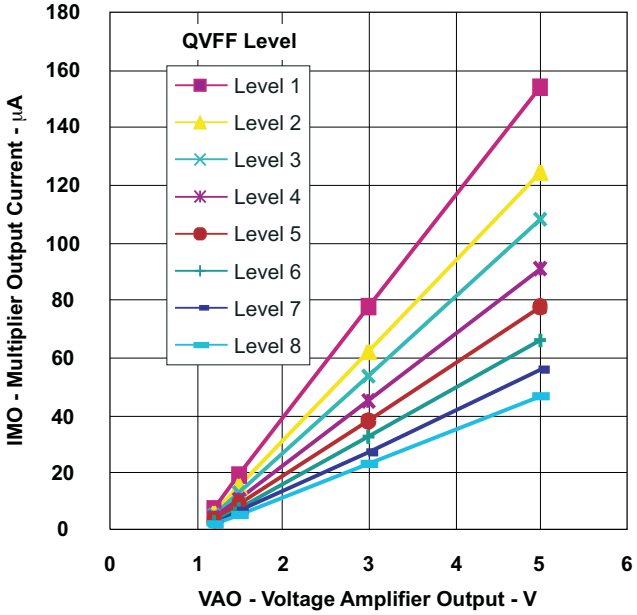


Figure 5.

MULTIPIER CONSTANT vs TEMPERATURE

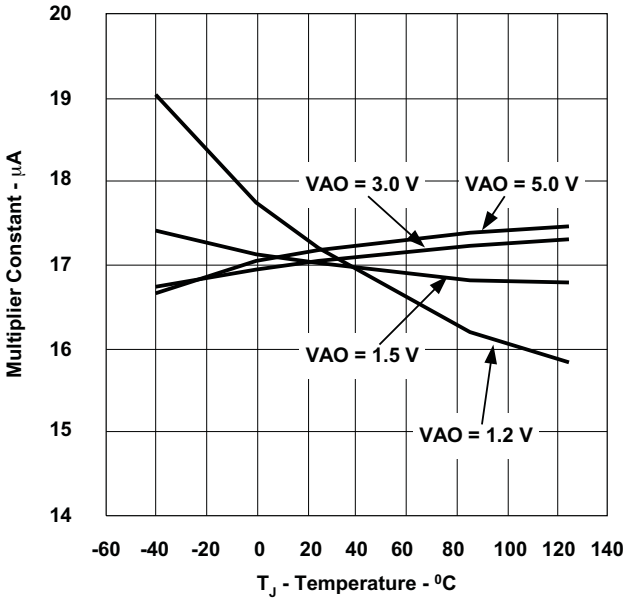


Figure 6.

I_{VINAC} BIAS CURRENT vs TEMPERATURE

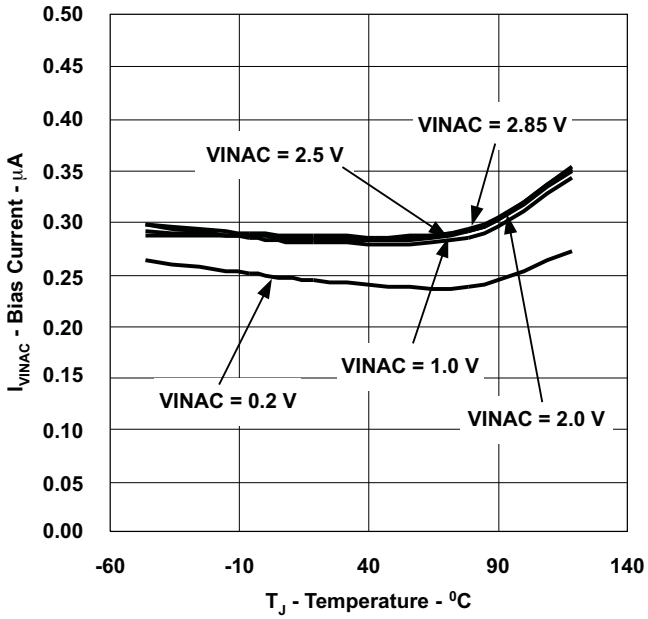


Figure 7.

SWITCHING FREQUENCY (normalized change) vs TEMPERATURE

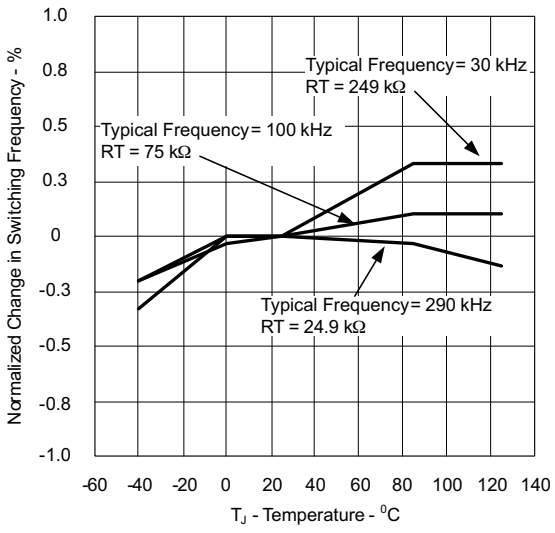


Figure 8.

TYPICAL CHARACTERISTICS (continued)

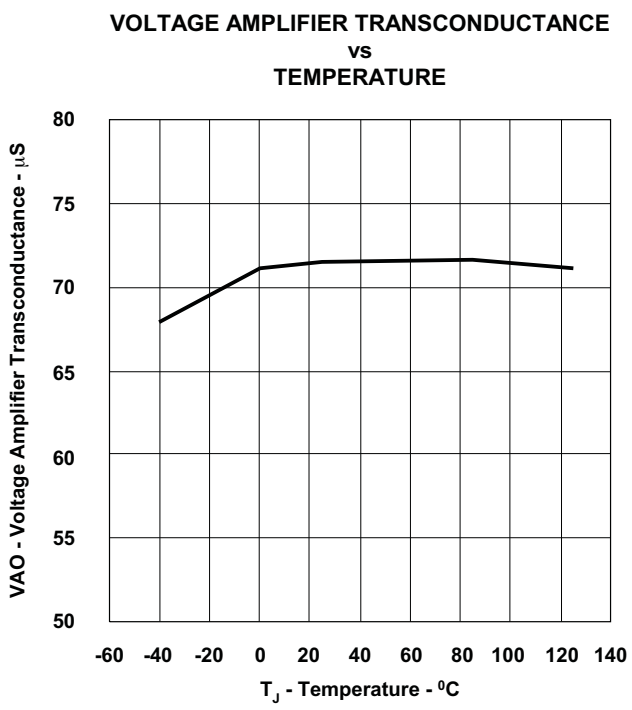


Figure 9.

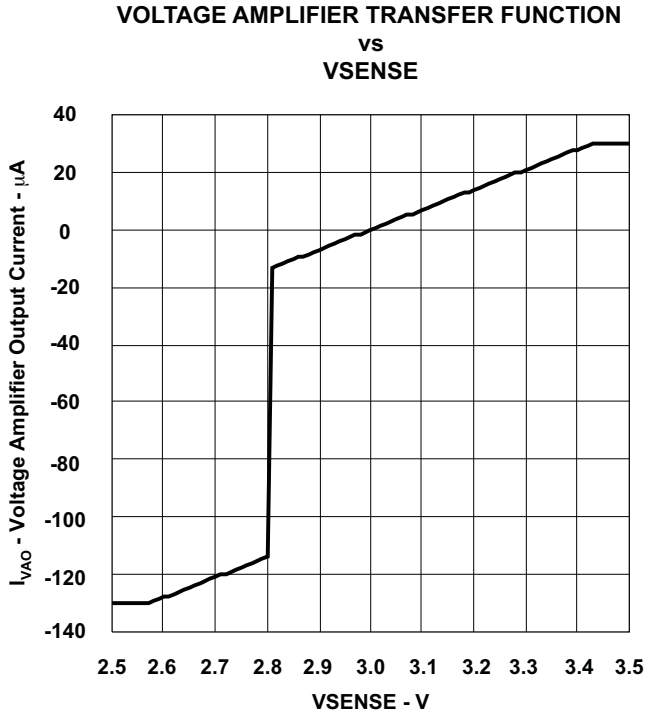


Figure 10.

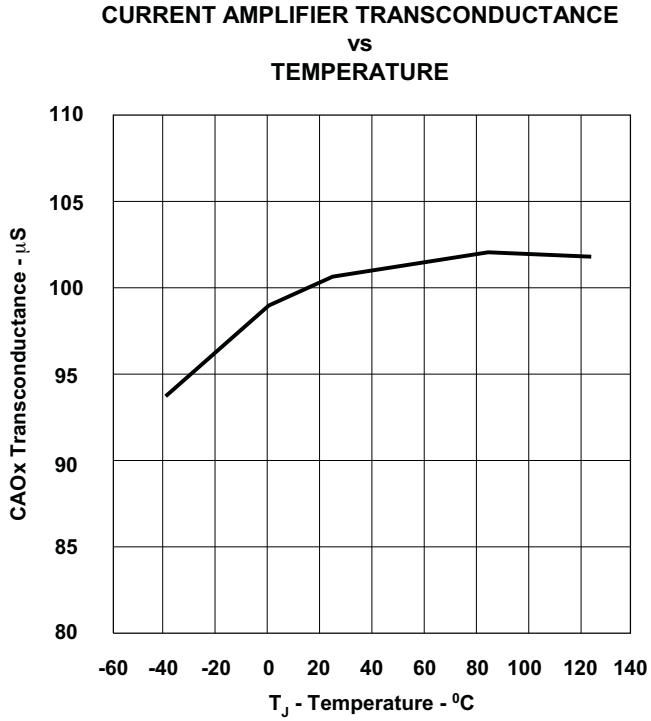


Figure 11.

TYPICAL CHARACTERISTICS (continued)

CAx INPUT OFFSET VOLTAGE vs TEMPERATURE (at 0.8 V common mode)

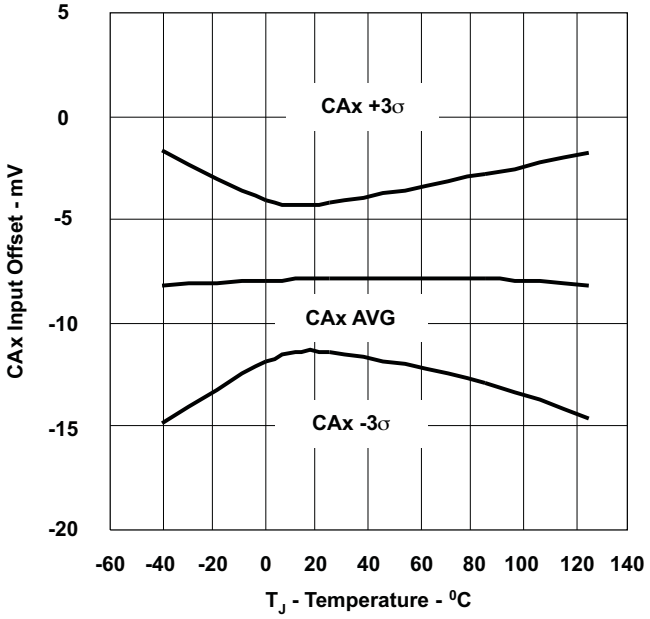


Figure 12.

CA1 TO CA2 RELATIVE OFFSET vs TEMPERATURE (at 0.8 V common mode)

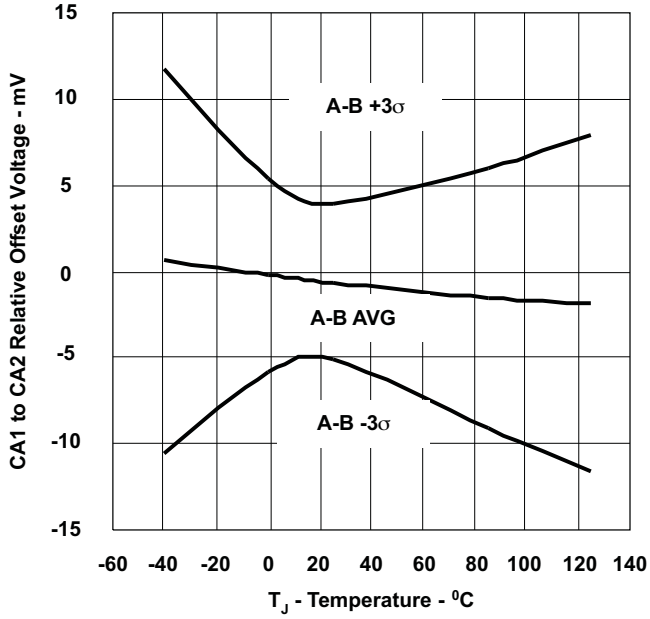


Figure 13.

CAx INPUT OFFSET VOLTAGE vs TEMPERATURE (at 2.0 V common mode)

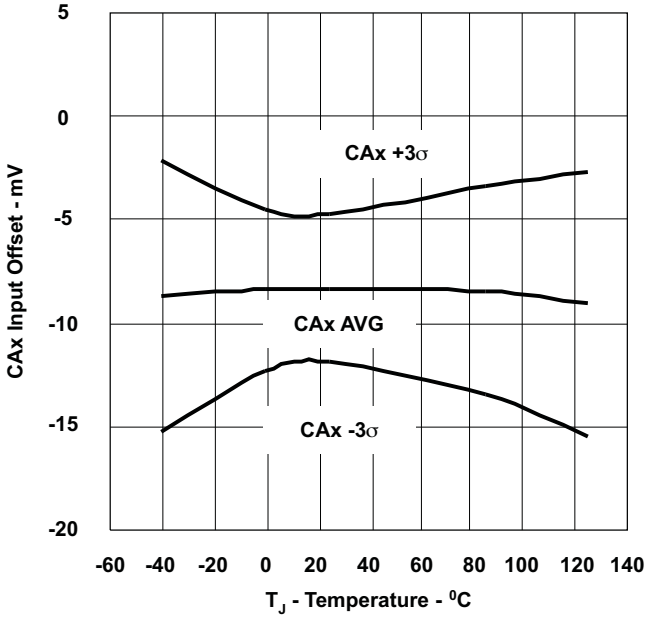


Figure 14.

CA1 TO CA2 RELATIVE OFFSET vs TEMPERATURE (at 2.0 V common mode)

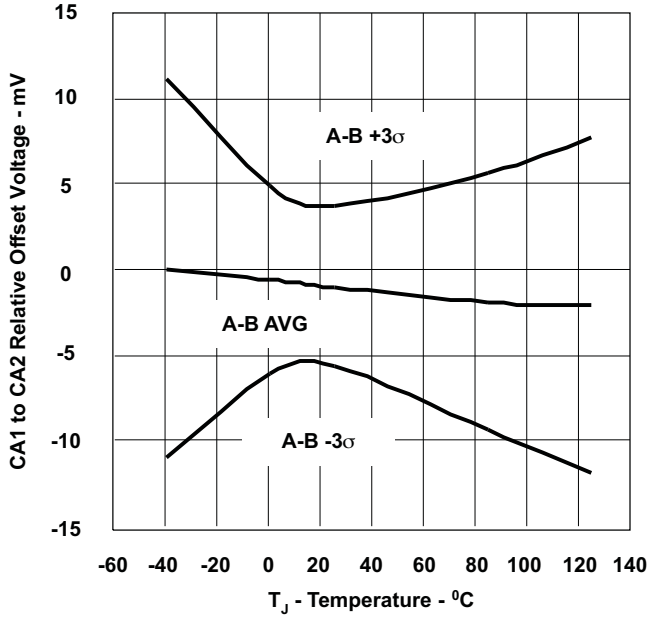


Figure 15.

TYPICAL CHARACTERISTICS (continued)

CAx INPUT OFFSET VOLTAGE vs TEMPERATURE (at 3.6 V common mode)

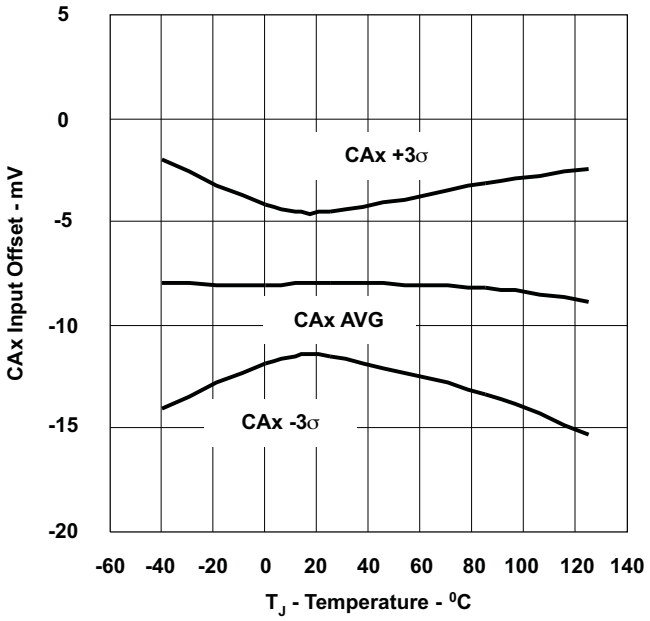


Figure 16.

CA1 TO CA2 RELATIVE OFFSET vs TEMPERATURE (at 3.6 V common mode)

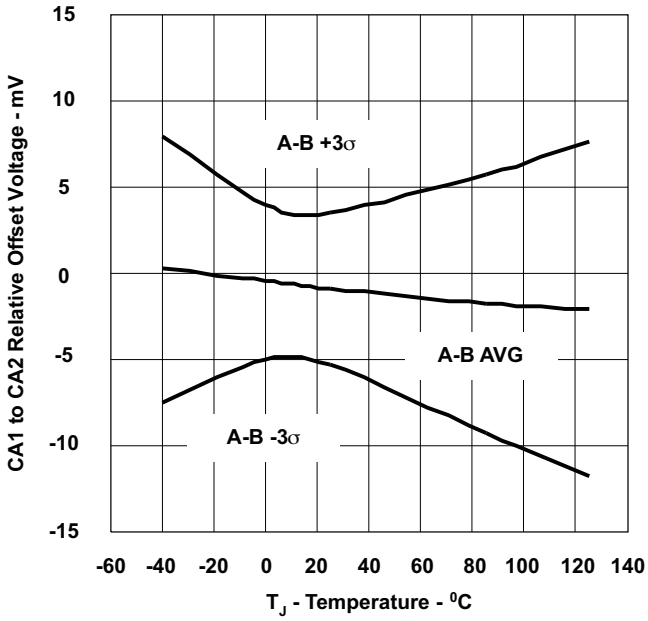


Figure 17.

APPLICATION INFORMATION

THEORY OF OPERATION

Interleaving

One of the main benefits from the 180° interleaving of phases is significant reductions in the high-frequency

180度相位交错的主要好处之一，就是减小了PFC预调节器的输入电流和流入PFC预调节器输出电容电流的高频纹波。与同功率级别的单相PFC调节器相比，输入电流纹波的减小可以减小EMI滤波器负担，也有助于减小EMI滤波器和输入电容的尺寸。同时，流入PFC输出电容电流的高频纹波的减小，也有助于减小输出电容的尺寸和成本。此外，随着各路的纹波和平均电流的减小，升压电感的尺寸也比单相设计的要小。

with reduced ripple and average current in each phase, the boost inductor size can be smaller than in a single-phase design [1].

由相位交错而来的纹波电流的减小通常被称作“纹波消除”，但严格来说，完全消除峰峰值只发生在50%占空比的两相系统。在不是50%占空比时，只在两相电流叠加的部分发生纹波消除。虽然如此，相比于同级别的单相PFC预调节器，这种两相交错的设计的纹波电波也有显著的减小。在输入输出端，交错纹波的频率都是两倍的PWM频率。

those of a 2-phase interleaved design are extraordinarily smaller [1]. Independent of ripple cancellation, the frequency of the interleaved ripple, at both the input and output, is 2 x f_{PWM}.

在输入端，180度交错的峰峰值纹波幅度是单相的1/2或更小。

在输出端，对于PWM占空比大于50%的，一个比根号2稍大的因数，180度交错减小了输出电容 上PFC产生的纹波电流有效值。

下面通过Erickson[2]的方法进行推导。

In a single-phase PFC pre-regulator, the total rms capacitor current contributed by the PFC stage at all duty-cycles can be shown to be approximated by:

$$i_{CRMS1\varphi} = \left(\frac{I_O}{\eta}\right)\sqrt{\left(\left(\frac{16V_O}{3\pi V_M}\right) - 1\eta^2\right)} \quad (1)$$

In a dual-phase interleaved PFC pre-regulator, the total rms capacitor current contributed by the PFC stage for D > 50% can be shown to be approximated by:

$$i_{CRMS2\varphi} = \left(\frac{I_O}{\eta}\right)\sqrt{\left(\left(\frac{16V_O}{6\pi V_M}\right) - 1\eta^2\right)} \quad (2)$$

In these equations, I_O = average PFC output load current, V_O = average PFC output voltage, V_M = peak of the input ac-line voltage, and η = efficiency of the PFC stage at these conditions. It can be seen that the quantity under the radical for $i_{Crms2\varphi}$ is slightly smaller than 1/2 of that under the radical for $i_{Crms1\varphi}$. The rms currents shown contain both the low-frequency and the high-frequency components of the PFC output current. Interleaving reduces the high-frequency component, but not the low-frequency component.

Programming the PWM Frequency and PWM频率和最大占空比的设置

The PWM frequency and maximum duty-cycle clamps for both GDx outputs of the UCC28070 are set through the selection of the resistors connected to the RT and DMAX pins, respectively. The selection of the RT resistor (R_{RT}) directly sets the PWM frequency (f_{PWM}).

$$R_{RT}\left(k\Omega\right)=\frac{7500}{f_{PWM}\left(kHz\right)} \tag{3}$$

Once R_{RT} has been determined, the D_{MAX} resistor (R_{DMX}) may be derived.

$$R_{DMX}=R_{RT}\times\left(2\times D_{MAX}-1\right) \tag{4}$$

where D_{MAX} is the desired maximum PWM duty-cycle.

Frequency Dithering (Magnitude and Rate) 频率抖动（幅度和速率）

Frequency dithering refers to modulating the switching frequency to achieve a reduction in conducted-EMI noise

频率抖动指的是调制开关频率来获得EMI噪声的减小。UCC28070实现了一种用相等时间在沿开关频率上每一点的三角波调制方法。从最小到最大的总的频率范围被定义为抖动幅度，并以由Rrt设置的额定开关频率Fpwm为中心点。例如，一个幅度为20hHz的抖动加在额定为100kHz的开关频率上，得到的频率范围就是100+/-10kHz。此外，由Rdmx设置的占空比钳位值在整个抖动频率范围内不变。

frequency range of 100 kHz ±10 kHz. Furthermore, the programmed duty-cycle clamp set by R_{DMX} remains constant at the programmed value across the entire range of the frequency dithering.

Fpwm频率值从最大达到最小再回到最大值的速率定义为抖动速率。例如，一个1kHz的抖动频率可线性的调制额定频率在每毫秒内从110kHz降到90kHz再回到110kHz。一种较好的初始设计是将抖动幅度设置为开关频率Fpwm的正负10%。大多数升压元件可接受在Fpwm上的这种误差。然后设计人员可以在此基础上迭代参考得到EMI抑制，元件误差和开路稳定性之间的最佳平衡关系。

compromise between EMI reduction, component tolerances, and loop stability.

抖动幅度由RDM接到GND的电阻设置。按下式计算可得RMD值。

equation:

$$R_{RDM}\left(k\Omega\right)=\frac{937.5}{f_{DM}\left(kHz\right)} \tag{5}$$

之后可由CDR接到GND的电容来设置抖动速率。电容值按下式算得

GND, or value calculated by the following equation:

$$C_{CDR}\left(pF\right)=66.7\times\left(\frac{R_{RDM}\left(k\Omega\right)}{f_{DR}\left(kHz\right)}\right) \tag{6}$$

频率抖动可按CDR脚拉高到大于5V或直接接到VREF(6V)并把风RDM直接接GND来完全禁止。（在抖动功能禁止时，如果没有一个低阻抗回路，RDM电阻相对较高的阻抗将会使系统开关噪声耦合到芯片的计时功能模块从而对计时模块产生干扰）

low impedance path when dithering is disabled.)

如果要使用一个外部频率来同步开关频率Fpwm和频率抖动幅度与速率，那此频率源要提供抖动幅度和速率而内部的抖动功能要禁止，以避免在同步时出现设计之外的状况。（详细介绍请见下一章）

to prevent undesired performance during synchronization. (See following section for more details.)

External Clock Synchronization 外部时钟同步

The UCC28070 has also been designed to be easily synchronized to almost any external frequency source. By

UCC28070也被设计成了很容易实现与外部频率源的同步。当把频率抖动功能禁止后，UCC28070的同步电路就开始工作，使内部振荡器同步到RDM引脚输入的脉冲波形。为了保证GDA和GDB输出之间180度的相位偏移，RDM引脚上的同步频率Fsync必须是两倍大的开关频率Fpwm。例如，如果想得到一个100kHz的开关频率，那么同步频率必须是200kHz。

is desired, the f_{SYNC} should be 200 kHz.

$$f_{PWM} = \frac{f_{SYNC}}{2} \tag{7}$$

为了内部振荡器不与同步功能冲突，Rrt的设置必须把内部振荡器频率设置在同步频率的10%或更小。

internal oscillator frequency at least 10% below the f_{SYNC}.

$$R_{RT}\left(k\Omega\right) = \frac{15000}{f_{SYNC}\left(kHz\right)} \times 1.1 \tag{8}$$

需要注意的是，由于PWM钳位电流与Rrt的直接关系，PWM调制器的增将会以Rrt为比例因子减小。必须要相应的对电流环进行调节。

made accordingly.

It must also be noted that the maximum duty cycle clamp programmability is affected during external synchronization. The internal timing circuitry responsible for setting the maximum duty cycle is initiated on the

同样要注意的，是在外部同步时，最大占空比的设置也会受到影响。内部定时电路负责在同步脉冲的下降沿设置最大占空比。因此，要根据同步脉冲宽度（Tsync）来选择Rdmx。

$$D_{SYNC} = t_{SYNC} \times f_{SYNC}$$ For use in R_{DMX} equation immediately below. (9)

$$R_{DMX}\left(k\Omega\right) = \left(\frac{15000}{f_{SYNC}\left(kHz\right)}\right) \times \left(2 \times D_{MAX} - 1 - D_{SYNC}\right) \tag{10}$$

Consequently to minimize the impact of the t_{SYNC} it is clearly advantageous to utilize the smallest synchronization pulse width feasible.

NOTE

When external synchronization is used, a propagation delay of approximately 50 ns to 100 ns exists between internal timing circuits and the SYNC signal's falling edge, which may result in reduced off-time at the highest of switching frequencies. Therefore, R_{DMX} should be adjusted downward slightly by (T_{SYNC}-0.1 µs)/T_{SYNC} to compensate. At lower SYNC frequencies, this delay becomes an insignificant fraction of the PWM period, and can be neglected.

Multi-phase Operation 多相运行

External synchronization also facilitates using more than 2 phases for interleaving. Multiple UCC28070s can easily be paralleled to add an even number of additional phases for higher-power applications. With appropriate phase-shifting of the synchronization signals, even more input and output ripple current cancellation can be obtained. (An odd number of phases can be accommodated if desired, but the ripple cancellation would not be

外部同步也便于2相以上的交错。多个UCC28070可很容易地并上一个甚至多个相位来作高功率应用。适当的同步信号相位偏移，可更多的消除输入输出纹波电流。（奇数相也可以设计，但纹波消除效果不佳）。对于4相、6相任意2n相（n为UCC28070的使用个数），每个控制器要接收到相位差为360/n的同步信号。在使用了两个控制器的4相应用中，SYNC1必须与SYNC2有180度相位差来获得最佳的纹波消除。6相应用中，SYNC1,SYNC2和SYNC3则两两之间相差120度，这样才能获得最佳纹波消除。

optimal ripple cancellation.

在一个多想交错系统中，每个电流环相互独立，但只有一个共同的电压环。为了维持单独的控制环，n个控制器之间所有的VSENE, VINAC, SS, IMO和VAO信号都是并联的。当电流源输出（SS，IMO，VAO）组合在一起，计算得的负载阻抗要以1/n进行调整，以维持作为单个控制的相同性能。

IMO, VAO), the calculated load impedances must be adjusted by 1/n to maintain the same performance as with a single controller.

Figure 18 图18展示了两个控制器作的4相90度交错PFC系统

VSENSE and VINAC Resistor Configuration VSENSE和VINAC电阻设置

The primary purpose of the VSENSE input is to provide the voltage feedback from the output to the voltage control loop. Thus, a traditional resistor-divider network needs to be sized and connected between the output

VSENSE输入的首要作用是为输出到电压控制环提供电压反馈。因此，需要一个电阻分压网络从输出端接到VSENSE与3V基准比较，来设置输出电压。

A unique aspect of the UCC28070 is the need to place the same resistor-divider network on the V_{IN} side of the

UCC28070的一个独特之处，是需要在电感的Vin侧接相同的电阻分压网格到VINAC脚。这为线性乘法器和电流合成器提供了输入与电压等比的监测信号。VINAC网络的实际阻值并不一定要和VSENSE网络的完全一致，但为了PFC正常运行，两个分压网络的衰减比值（Kr）必须一致。

proper PFC operation.

$$k_R = \frac{R_B}{(R_A + R_B)} \quad (11)$$

在噪声环境中，在VSENSE和VINAC输入上加一个小滤波电容可以很好地避免过大的噪声导致的不稳定。如果使用了滤波电容，那在VSENSE输入端的RC时间常数不要超过100us，避免输出瞬态响应的延迟。VINAC输入端的时间常数也不能超过100us，避免波形过零的降低。通常3/fpwm的时间常数就足够滤掉VSENSE和VINAC上的噪声。为了在特殊的应用中获得最佳的滤波效果，一些设计和实验是必要的。

zero-crossings. Usually, a time constant of $3/f_{PWM}$ is adequate to filter out typical noise on VSENSE and VINAC. Some design and test iteration may be required to find the optimal amount of filtering required in a particular application.

VSENSE and VINAC Open Circuit Protection VSENSE和VINAC开环保护

VSENSE和VINAC被设计成内部250nA电流灌入以确保在任一引脚出现开环时，电压不会变得不确定，同时UCC28070也能处在一个相对安全的工作状态。

operating mode.

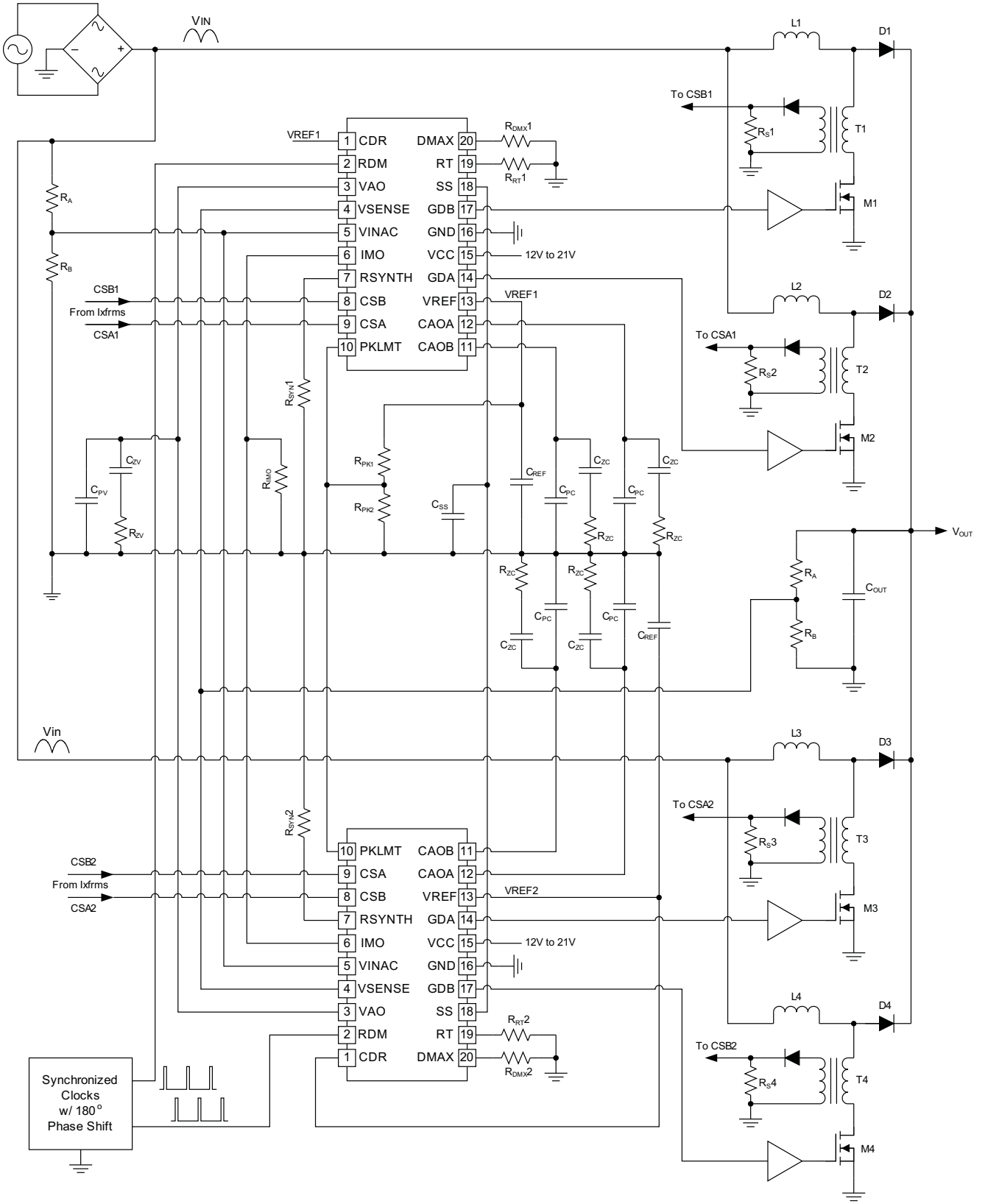


Figure 18. Simplified Four-Phase Application Diagram Using Two UCC28070

Current Synthesizer 电流合成器

UCC28070最大的一个创新是电流合成电路，它能同步监测导通时间采样和关断时间的下斜坡仿真的瞬时电感电流。

off-time down-slope emulation.

During the on-time of the GDA and GDB outputs, the inductor current is recorded at the CSA and CSB pins respectively via the current transformer network in each output phase. Meanwhile, the continuous monitoring of the input and output voltage via the VINAC and VSENSE pins permits the UCC28070 to internally recreate the

在GDA和GDB的导通时间内，通过每一相输出的电流互感器分别在CSA和CSB记录下电感电流。同时，通过VINAC和VSENSE引脚对输入输出电压的连续监测，让UCC28070在内部分别再现每相输出关断时间的下降斜坡。通过选择RSYNTH电阻的值（按下面的公式算得），内部响应可被调整以适应不同场合的电感变化。

During inrush surge events at power-up and ac drop-out recovery, VSENSE < VINAC, so the synthesized down

在启动和AC跌落恢复时的浪涌中，VSENSE<VINAC，所以合成的下降斜坡为零。在这种情况下，合成的电感电流将保持高于IMO基准，同时电流环使占空比为零。这样可以避免浪涌时MOSFET过压。一旦VINAC下降到小于VSENSE后，占空比开始增加直到恢复至稳定状态。

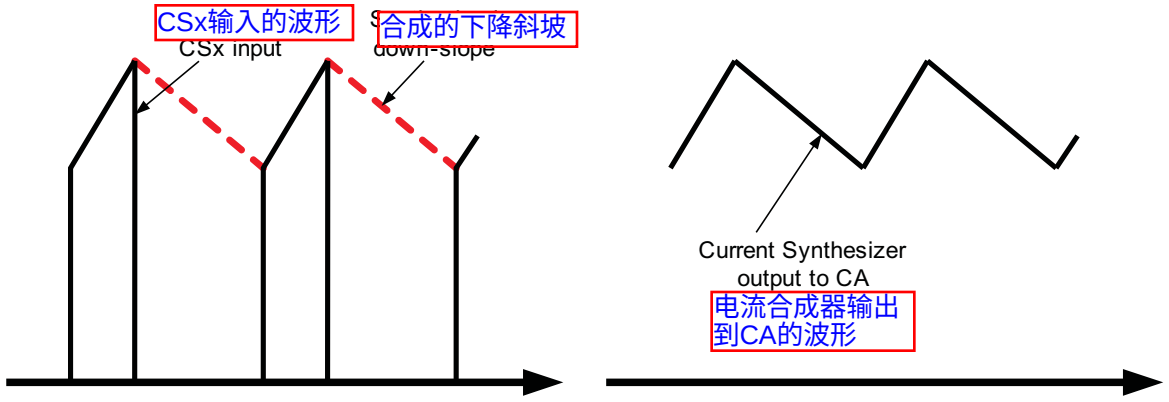


Figure 19. Inductor Current's Down Slope

$$R_{SYN}\left(k\Omega\right)=\frac{\left(10\times N_{CT}\times L_B\left(\mu H\right)\times k_R\right)}{R_S\left(\Omega\right)} \quad (12)$$

Variables

- L_B = Nominal Zero-Bias Boost Inductance (μH) 零偏置升压电感（uH）
- R_S = Sense Resistor (Ω), 检测电阻（R）
- N_{CT} = Current-sense Transformer turns ratio, 电流互感器匝比
- $k_R = R_B/(R_A+R_B)$ = the resistor-divider attenuation at the VSENSE and VINAC pins.
  VSENSE和VINAC引脚上的电阻分压比

Programmable Peak Current Limit 峰值电流限制

The UCC28070 has been designed with a programmable cycle-by-cycle peak current limit dedicated to disabling either GDA or GDB output whenever the corresponding current-sense input (CSA or CSB respectively) rises above 3.6 V.

UCC28070设计了一个可程控的逐周期的峰值电流限制，用于在相应电流检测引脚（CSA或CSB）输入电压超过在PKLMT脚上设置的值时禁止GDA或GDB输出。一旦其中一个输出通过峰值电流限制被禁止，输出就会一直被禁止直到下一个时钟周期才开始一个新的PWM周期。PKLMT的电压设置范围达到4V以上，以完全利用电流检测信号平均3V的范围，然而要注意的是，电流放大的线性度开始压缩大于3.6V。

A resistive divider network from VREF to GND can easily program the peak current limit at PKLMT. VREF must source less than 2 mA to avoid pulling down the 6-V reference voltage. A load of less than 0.5 mA is recommended. However, if the impedance at PKLMT is very high, a small bypass capacitor is recommended to avoid operational problems in high-noise environments.

一个从VREF到GND的电阻分压网络可方便的在PKLMT设置峰值电流，VREF提供的总电流要小于2mA以避免6V基准电压被拉低。建议使用的负载小于0.5mA。但是如果PKLMT上的阻抗非常大，则建议在PKLMT上接一个小滤波电容，避免在重噪声环境中出现问题。

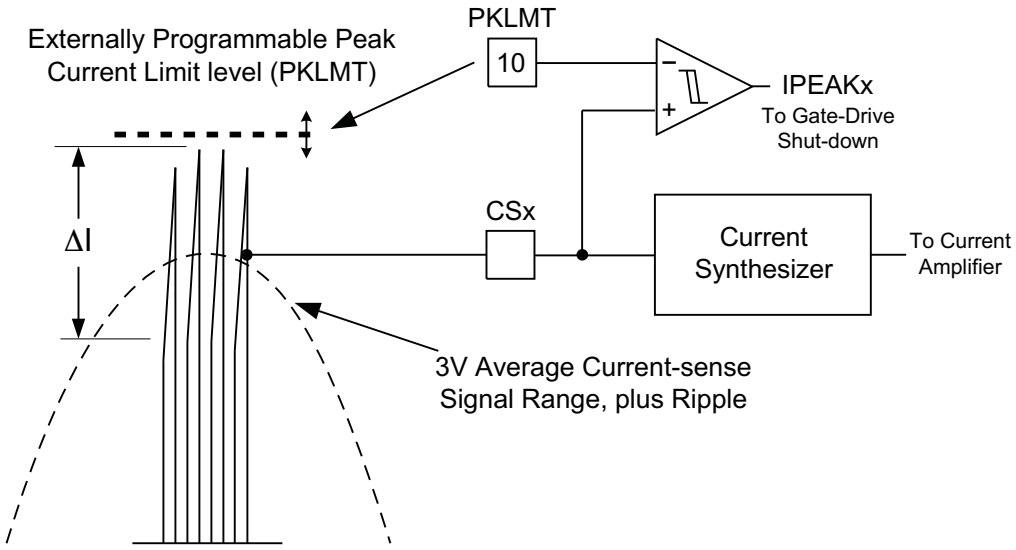


Figure 20. Externally Programmable Peak Current Limit

Linear Multiplier 线性乘法器

The multiplier of the UCC28070 generates a reference current which represents the desired wave shape and proportional amplitude of the ac input current. This current is converted to a reference voltage signal by the R_{IMO}

UCC28070的乘法器产生一个基准电流，此电流表现为ac输入电流的预期波形和等比幅值。此电流通过Rimo电阻转化为一个电压信号，以此电压值来与电流检测信号电压相比较。乘法器的瞬时电流与整流桥，输入电压Vvinac和电压误差放大器输出Vvao相关。Vvinca信号传递了三个信号给乘法器。

1. 输入电压的完整波形（典型的正弦波）
2. 线周期上任意点的瞬时输入电压大小
3. 输入电压的RMS

Vvao信号体现了PFC预调节器的总输出功率

A major innovation in the UCC28070 multiplier architecture is the internal quantized V_{RMS} feed-forward (Q_{VFF}) circuitry, which eliminates the requirement for external filtering of the VINAC signal and the subsequent slow

UCC28070乘法器的主要创新，是内部量化电压前馈电路，它消除了对VINAC信号的外部滤波和随之出现的对线路瞬时变化的过慢响应要求。一种独特的电路算法检测Vvinac峰值经过7个阈值的变化并产生一个等效为八个Qvff范围为中心的VFF。这些边界范围的扩大和升高Vin来维持大概相等的百分比增量。这八个Qvff等级被分开来以适应85-265的宽电压范围。

V_{RMS}.

A great benefit of the Q... architecture is that the fixed k... factors eliminate any contribution to distortion of the ... threshold or containing mild ringing or distortion. The Q_{VFF} architecture requires that the input voltage be largely sinusoidal, and relies on detecting zero-crossings to adjust Q_{VFF} downward on decreasing input voltage. Zero-crossings are defined as V_{VINAC} falling below 0.7 V for at least 50 µs typically.

Qvff构造的一个非常大的好处，是合适的Kvff因子消除了对乘法器输出的影响，不像一个外部滤波的VINAC信号不可避免地包含了二次谐波畸变成分。此外，Qvff算法可对输入RMS电压的上升或下降的变化快速响应，从而使传递到PFC输出的不稳定最小化。在等级间阈值的5%滞后有助于避免在VINAC电压峰值在接近某个阈值时或包含的轻微振荡或失真而带来的Qvff的级间抖振。Qvff构造要求输出电压接近正弦波，并根据过零检测来调节输出电压下降时Qvff的下降。过零点通常定义为VINAC下降到0.7V以下并维持至少50us.

Table 1 reflects the relationship between the various VINAC peak voltages and the corresponding k_{VFF} terms for the multiplier equation. 表1反映了不同的VINAC峰值电压与相应的Kvff的关系

Table 1. VINAC Peak Voltages

LEVEL	V_{VINAC} PEAK VOLTAGE	k_{VFF} (V^2)	V_{IN} PEAK VOLTAGE (1)
8	2.60 V ≤ $V_{VINAC(pk)}$	3.857	> 345 V
7	2.25 V ≤ $V_{VINAC(pk)}$ < 2.60 V	2.922	300 V to 345 V
6	1.95 V ≤ $V_{VINAC(pk)}$ < 2.25 V	2.199	260 V to 300 V
5	1.65 V ≤ $V_{VINAC(pk)}$ < 1.95 V	1.604	220 V to 260 V
4	1.40 V ≤ $V_{VINAC(pk)}$ < 1.65 V	1.156	187 V to 220 V
3	1.20 V ≤ $V_{VINAC(pk)}$ < 1.40 V	0.839	160 V to 187 V
2	1.00 V ≤ $V_{VINAC(pk)}$ < 1.20 V	0.600	133 V to 160 V
1	$V_{VINAC(pk)}$ ≤ 1.00 V	0.398	< 133 V

(1) The V_{IN} peak voltage boundary values listed above are calculated based on a 400-V PFC output voltage and the use of a matched resistor-divider network (k_R = 3 V/400 V = 0.0075) on VINAC and VSENSE (as required for current synthesis). When V_{OUT} is designed to be higher or lower than 400 V, k_R = 3 V/V_{OUT}, and the V_{IN} peak voltage boundary values for each Q_{VFF} level adjust to $V_{VINAC(pk)}/k_R$.

Vin峰值电压边界值是在PFC输出400V，VINAC和VSENSE分压网络的分压比为Kr=3/400=0.0075时计算而得的。当Vout要设计为比400V不一样时，Kr=3/Vout，并且Vin的峰值电压边界值要按Vinac(pk)/Kr重新计算。

The multiplier output current I_{IMO} for any line and load condition can thus be determined by the equation

$$I_{IMO} = \frac{17\mu A \times (V_{VINAC}) \times (V_{VAO} - 1)}{k_{VFF}} \quad (13)$$

乘法器输出电流Iimo在任意线路和负载条件时可按下式计算得到

Because the k_{VFF} value represents the scaled V_{VINAC}^2 at the center of a level, V_{VAO} will adjust slightly upwards or downwards to compensate for the difference. This is automatically accomplished by the voltage loop control when V_{IN} varies, both within a level and after a transition between levels.

因为Kvff的值在一个电压级别中心表现为与Vrms平方等比，在VINACpk比Qvff电压范围中心值低或高时Vvao将轻微地向上或向下调节，来为这此差异作补偿。这在Vin变化时由电压环控制自动完成。

The output of the voltage amplifier, VAO, is clamped at 5.0 V, which represents the maximum PFC output power maximum input power allowed (and, as a consequence, limits maximum output power).

电压误差放大器的输出被钳位在5V，这个5V体现为PFC输出的最大功率。这个值通常用来计算在IMO引脚的最大基准电流，同时为输出输入功率作限制（同时也就限制了最大输出功率）。

Unlike a continuous V_{ff} situation, where maximum input power is a fixed power at any V_{RMS} input, the discrete such level.

不像Vff连续的情况，最大输入功率在任何Vrms输入时都是一个固定的，不连续的Qvff级别允许在每个级别中限制边界内最大输入功率随输入VRMS变化而变化。

The lowest maximum power limit occurs at the VINAC voltage of 0.76 V, while the highest maximum power limit P_{IN} is always less than $P_{IN(max)}$, falling linearly to zero with decreasing input voltage.

在VINAC电压为0.76V时最大功率限制值最低，而最大功率发生在级别1到级别2的上升阈值处。这种模式在每个级别的过渡阈值处重复，同时注意下降阈值是上升阈值的95%。在VINAC=0.76V以下时，Pin通常都小于Pin(max)，随着输入电压的减小线性下降到零。

For example, to design for the lowest maximum power allowable, determine the maximum steady-state (average) output power required of the PFC pre-regulator and add some additional percentage to account for line drop-out the expected efficiency factor to find the lowest maximum input power allowable.

例如，为了设计允许最低的最大功率，要确定需要的PFC最大稳定（平均）输出功率和线路从跌落恢复到正常供电时增加的一些额外功率（输出功率的10%或20%）。再用预期的效率因数来算出最低的最大输入功率，如下式：

$$P_{IN(max)} = \frac{1.10 \times P_{OUT(max)}}{\eta} \quad (14)$$

在Pin(max)的阈值处，一个额定输出为400V的系统中，VINAC=0.76V，因此Qvff=0.398V，输入Vac=73Vrms（算上整流桥的2V压降）

$$\text{Thus } I_{IN(rms)} = \frac{P_{IN(max)}}{73 V_{RMS}}, \text{ and } I_{IN(pk)} = 1.414 \times I_{IN(rms)} \quad (15)$$

这个Iin(pk)的值是在线路电压峰值时流过升压电感的合成电流。每个电感电流都由电流互感器CT检测得到。若有相等的电流流过每个交错相，在每个电流检测输入脚（CSA和CSB）上的电压信号经过一个检流电阻按（1/2）*Iin(pk) *Rs/Nct计算得到3V，其中Rs是检流电阻，Nct是CT的匝比。

developed across a sense resistor selected to generate ~3 V based on (1/2) x $I_{IN(pk)}$ x R_S/N_{CT}, where R_S is the current sense resistor and N_{CT} is the CT turns-ratio.

I_{IMO} is then calculated at that same lowest maximum-power point, as

然后就可按下式算得IMO电流大小

$$I_{IMO(max)} = 17\mu A \times \frac{(0.76V)(5V - 1V)}{0.398} = 130\mu A \quad (16)$$

R_{IMO} is selected such that: Rimo按下式选择

$$R_{IMO} \times I_{IMO(max)} = \left(\frac{1}{2}\right) \times I_{IN(pk)} \times \frac{R_S}{N_{CT}} \quad (17)$$

Therefore: 则有

$$R_{IMO} = \frac{\left(\left(\frac{1}{2}\right) \times I_{IN(pk)} \times R_S\right)}{\left(N_{CT} \times I_{IMO(max)}\right)} \quad (18)$$

At the increasing side of the lev 在级别1到级别2阈值的上升方向，要注意在低压线路上IMO电流会有更大的输入电流 d allow higher input currents at low-line:

$$I_{IMO(L1-L2)} = 17\mu A \times \frac{(1.0V)(5V - 1V)}{0.398} = 171\mu A \quad (19)$$

然而，如果在应用中有要求，此电流可以很容易地通过UCC28070的峰值电流限制功能来限制 UCC28070 if required by the power stage design.

The same procedure can be used to find the lowest and highest input power limits at each of the Q_{VFF} level transition thresholds. At higher line voltages, where the average current with inductor ripple is traditionally below

同理，可得到每个Qvff级别过渡阈值处的最小和最大输入功率限制。在较高的线压上，电感纹波平均电流通过小于IPKMT的阈值，可观察到最大输入功率充分变化，但输入电流一定会比此功率级别所允许的最大电流小。

be below the maximum acceptable current levels of the power stage.

The performance of the multiplier in the UCC28070 has been significantly enhanced when compared to previous generation PFC controllers, with high linearity and accuracy over most of the input ranges. The accuracy is at its worst as V_{VAO} approaches 1 V because the error of the (V_{VAO}-1) subtraction increases and begins to distort the IMO reference current to a greater degree.

相比于传统的PFC控制器，UCC28070的乘法器性能有了很大的提升，在大多数输入范围内有极高的线性度和准确度。精度最差发生在VAO接近1V时，因为此时（VAO-1)的误差增大，并且IMO基准电流开始在更大范围内扭曲。

Enhanced Transient Response (VA Slew-Rate Correction) 增强的瞬态响应

Due to the low voltage loop bandwidth required to maintain proper PFC and ignore the slight 120-Hz ripple on the output, the response of ordinary controllers to input voltage and load transients will also be slow. However, the Q_{VFF} function effectively handles the line transient response with the exception of any minor adjustments

由于低电压环带宽要维持适当的PFC并魅力输出120Hz轻微纹波，通常控制器对输入电压和负载的瞬态响应也会变慢。然而，Qvff功能高效的处理了线路瞬态响应，除了一个Qvff级别内的任意微波调整需求。 负载瞬态在另一方面可由电压环处理，因此，UCC28070通过一个在VSENSE电压低于规定值（2.79V）的93%以下时附加的100uA电流来拉高电压放大器的输出，提高了瞬态响应。在软启动周期中，当VSENSE从0.75V的PFC使能阈值开始斜坡上升时，100uA的校正电流源被禁止，以保证输出电压和电流在软启动过程中可控地缓慢上升。

Voltage Biasing (VCC and VREF) 电压偏置（VCC和VREF)

The UCC28070 operates within a VCC bias supply range of 10 V to 21 V. An Under-Voltage Lock-Out (UVLO)

UCC28070由范围从10到21V的VCC电压供电。一个欠压锁定阈值使在VCC>10.2V之后才能使PFC工作，1V的滞后可保证从低规格偏置源稳定启动。在VCC上内部一个类似齐纳管的25V钳位只能用来保护芯片不受偏置源的浪涌损坏，一定不能当成一个电流限制调节器使用。

At minimum, a 0.1-uF ceramic bypass capacitor must be applied from VCC to GND close to the device pins to

至少用一个0.1uf的陶瓷电容在靠近引脚处从VCC接到GND，来对偏置源滤波。根据Icc峰值电流幅值和为了最大限度的减小VCC上的电压纹波，可能需要一个更大的电容。

为了UVLO能平滑过渡，同时为了尽快得到稳定的6V基准电压，VREF输出在VCC超过8V时就被使能了。

The VREF circuitry is designed to provide the biasing of all internal control circuits and for limited use externally

VREF电路为芯片内部所有的控制电路提供偏置电压，同时也作外部的使用（有限制）。VREF必须要挨着引脚处接一个至少0.22nF的陶瓷电容到GND来保护电路稳定。VREF的外部负载电流要限制在2mA以内，否则可能会将基准电压拉低。

PFC Enable and Disable PFC使能和禁止

The UCC28070 contains two independent circuits dedicated to disabling the GDx outputs based on the biasing conditions of the VSENSE or SS pins. The first circuit which monitors the V_{VSENSE}, is the traditional PFC Enable that holds off soft-start and the overall PFC function until the output has pre-charged to ~25%. Prior to V_{VSENSE} reaching 0.75 V, almost all of the internal circuitry is disabled. Once V_{VSENSE} reaches 0.75 V and VAO < 0.75 V, the oscillator, multiplier, and current synthesizer are enabled and the SS circuitry begins to ramp up the voltage on the SS pin. The second circuit provides an external interface to emulate an internal fault condition to disable the GDx output without fully disabling the voltage loop and multiplier. By externally pulling the SS pin below 0.6 V, the GDx outputs are immediately disabled and held low. Assuming no other fault conditions are present, normal PWM operation resumes when the external SS pull-down is released. It must be noted that the external pull-down needs to be sized large enough to override the internal 1.5-mA adaptive SS pull-up once the SS voltage falls below the disable threshold. It is recommended that a MOSFET with less than 100-Ω $R_{DS(on)}$ resistance be used to ensure the SS pin is held adequately below the disable threshold.

基于VSENSE或SS引脚的偏置条件，UCC28070有两个相互独立的电路来控制禁止GDx的输出。第一个电路对VSENSE监测，是传统的PFC使能方式，在输出被预充电到25%之前将保持软启动和所有PFC功能关闭。为了优先使VSENSE达到0.75V，几乎所有内部电路都被禁止。一旦VSENSE达到0.75V而VAO<0.75V，振荡器、乘法器、和电流合成器被使能，同时SS电路将SS引脚电压斜坡拉升。第二个电路提供一个外部端口模拟内部故障状态来禁止GDx输出，而不用完全禁止电压环和乘法器。当外部将SS引脚拉低到0.6V以下时，GDx输出会被立即禁止并保持低电压。假设没有其它的故障状态出现，在外部SS的拉低状态解除后PWM会恢复正常。要注意的是，一旦SS被拉低到阈值以下，外部的拉低能力要足够大以抵消内部1.5mA电流造成SS上升的电压。用一个Rds(on)小于100R的MOSFET可以确保SS引脚维持在禁止阈值以下。

Adaptive Soft Start 自适应软启动

In order to maintain a controlled power up, the UCC28070 has been designed with an adaptive soft-start function that overrides the internal reference voltage with a controlled voltage ramp during power up. On initial power up, once V_{VSENSE} exceeds the 0.75 V enable threshold (V_{EN}), the internal pull-down on the SS pin is released, and

为了维持上电可控，UCC28070设计了一个自适应软启动功能，在上电过程中它能无视内部基准电压而电压上升是受控的。在刚上电时，一旦VSENSE超过0.75V的使能阈值（Ven），内部对SS引脚的拉低就释放，同时1.5mA的自适应软启动电流源工作。这个1.5mA电流几乎是立即将SS引脚拉高到0.75V，从而绕开了从SS引脚0V开始上升到规定电压时的初始的25%的死区时间。一旦SS引脚电压达到VSENSE，10uA的软启动电流（Iss）开始接管工作。这样，通过下式选择软启动电容（Css）的值，就能方便高效的设置了软启动时间。

$$t_{SS} = C_{SS} \times \left(\frac{2.25V}{10\mu A} \right) \tag{20}$$

Often, a system restart is desired following a brief shut-down. In such a case, VSENSE may still have substantial voltage if V_{OUT} has not fully discharged or if high line has peak charged C_{OUT}. To eliminate the delay caused by

通常，系统要短暂停机后重启。这种情况下，如果Vout还没有被完全放电或高压线将Cout充电到了峰值，VSENSE可能依然还有电压。为了消除Css只用15uA电流从0V充电到VSENSE的延时，同时为了最大限度减小任何即将发生的输出电压凹陷，自适应软启动用一个1.5mA电流将Css快速充电到VSENSE，在10uA电流源控制Vss软启动上升率之后 。这种情况下，Tss可由下式得

$$t_{SS} = C_{SS} \times \left(\frac{3V - V_{VSENSE0}}{10\mu A} \right) \tag{21}$$

where $V_{VSENSE0}$ 是软启动或重启时在VSENSE的初始电压

NOTE

为了软启动的效率和避免Vout上的过冲，SS的上升必须要比电压环控制响应要慢。选用Css>=Cvz来保证

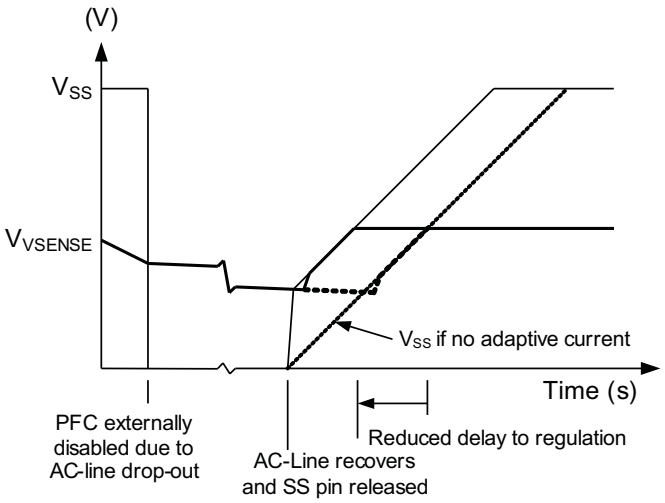


Figure 21. Soft-Start Ramp Rate

PFC Start-Up Hold Off PFC启动推迟

An additional feature designed into the UCC28070 is the “Start-Up Hold Off” logic that prevents the device from initiating a soft-start cycle until the VAO is below the zero-power threshold (0.75 V). This feature ensures that the

此功能可以防止芯片开始软启动周期，直到VAO低于零功率阈值（0.75V）以下。它能保证软启动周期将从零功率和零占空比周期开始，避免由于VAO补偿网络存留的电荷造成任何潜在的浪涌。

Output Over-Voltage Protection (OVP) 输出过压保护

Because of the high voltage output and a limited design margin on the output capacitor, output over-voltage protection is essential for PFC circuits. The UCC28070 implements OVP through the continuous monitoring of

因为输出电容的高压输出和有限的设计裕量，对于PFC电路来说输出过压保护是必不可少的。UCC28070通过连续监测VSENSE电压来实现过压保护。在VSENSE电压上升超过规定值（3.18V）的106%时，GDx输出直接被禁止避免输出电压过高。同时CAOx输出被拉低以保证在OVP故障排除后由0%占空比恢复启动。当VSENSE电压低于3.08V后，PWM恢复正常工作。

Zero-Power Detection 零功率检测

In order to prevent undesired performance under no-load and near no-load conditions, the UCC28070 zero-power detection comparator is designed to disable both GDA and GDB output in the event the VAO voltage

为了避免空载或接近空载时出现设计之外的状态，UCC28070的零功率检测比较器在VAO电压低于0.75V以下时禁止GDA和GDB输出。150mV的滞后保证了输出始终被禁止，直到VAO上升到乘法器的线性范围内（VAO>=0.9V）

Thermal Shutdown 过温保护

In order to protect the power supplies from silicon failures at excessive temperatures, the UCC28070 has an internal temperature-sensing comparator that shuts down nearly all of the internal circuitry, and disables the GDA

为了避免功率电源在过高的温度状态下失效，UCC28070有一个内部温度检测比较器，在温度超过160度时可以关断几乎所有内部电路，并禁止GDA和GDB输出。当温度下降到140度以下后，芯片通过软启动恢复正常工作。

Current Loop Compensation 电流环补偿

The UCC28070 incorporates two identical and independent transconductance-type current-error amplifiers (one for each phase) with which to control the shaping of the PFC input current waveform. The current-error amplifier (CA) forms the heart of the embedded current control loop of the boost PFC pre-regulator, and is compensated

UCC28070合并了两个一样的并相互独立的跨导型电流误差放大器（每相一个），用来控制PFC输入电流波形。电流误差放大器构成了升压PFC预调节器的钳入式电流控制环的核心，并用常见的方式为环路稳定作补偿。给A相的CA输出是CAOA，B相的是CAOB。

In a boost PFC pre-regulator, the current control loop comprises the boost power plant stage, the current sensing

在升压PFC预调节器中，电流控制环包括功率升压阶段，电流检测电路，波形基准，PWM阶段，和CA补偿部分。CA将平均升压电感电流与来自乘法器的波形基准比较，得到一个与此差等比的输出电流。

This CA output current flows through the impedance of the compensation network generating an output voltage, V_{CAO}, which is then compared with a periodic voltage ramp to generate the PWM signal necessary to achieve PFC.

这个CA的输出电流接着通过补偿网络的阻抗产生一个输出电压Vcao，然后与一个周期性的斜坡信号比较产生PWM信号从而实现PFC

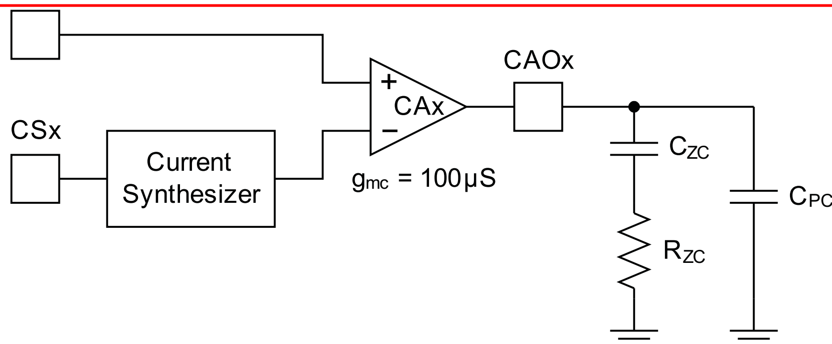


Figure 22. Current Error Amplifier With Type II Compensation

在频率高于LC谐振又低于Fpwm时，升压阶段包含电感电流的小信号模型如下式：

includes current sensing, can be simplified to:

$$\frac{v_{RS}}{v_{CA}} = \frac{Vout \times R_S / N_{CT}}{\Delta V_{RMP} \times k_{SYNC} \times s \times L_B} \quad (22)$$

where L_B = 升压电感的中值 R_S = CT检测电阻, N_{CT} = CT匝比 V_{OUT} = 平均输出电压 voltage, $\Delta V_{RMP} = 4V_{pk\text{-}pk}$ PWM电压上升幅值, k_{SYNC} = 斜坡衰减系数 (if PWM frequency is 如果PWM信号来自外部同步信号 $k_{SYNC} = 1$ otherwise), s = 拉普拉斯复变量

An $R_{ZC}C_{ZC}$ network is introduced on CAOx to obtain high gain for the low-frequency content of the inductor current signal, but reduced flat gain above the zero frequency out to f_{PWM} to attenuate the high-frequency switching ripple content of the signal (thus averaging it).

一个RzcCzc网络在CAOx上被引入，为电感电流信号的低步部分提供高增益，减小了在零频率点上到Fpwm的平坦增益，以减少高频信号的开关纹波成分。

The switching ripple voltage considered "negligible" ripple. 开关纹波电压要减小到ΔVrmp幅值的1/10以下以使其能被忽略

Thus, CAOx gain at f_{PWM} is: 则，CAOx在Fpwm的增益为

$$g_{mc}Rzc \le \frac{\Delta V_{RMP} \times k_{SYNC} / 10}{\Delta I_{LB} \times R_S / N_{CT}} \quad (23)$$

where ΔI_{LB} 是在升压电感上峰峰值纹波电流的最大值 and g_{mc} 是CA的跨导，100uS the CA, 100 µS.

$$Rzc \le \frac{4V \times N_{CT}}{10 \times 100\mu S \times \Delta I_{LB} \times R_S} \quad (24)$$

The current-loop cross-over frequency is then found by equating the open loop gain to 1 and solving for f_{CXO}: 电流环的穿越频率可由下式得

$$f_{CXO} = \frac{Vout \times R_S / N_{CT}}{\Delta V_{RMP} \times k_{SYNC} \times 2\pi \times L_B} \times g_{mc}Rzc \quad (25)$$

C_{CZ} is then determined by setting $f_{ZC} = f_{CXO} = 1/(2\pi x R_{ZC} x C_{ZC})$ and solving for C_{ZC}. At $f_{ZC} = f_{CXO}$, a phase margin of 45° is obtained at f_{CXO}. Greater phase margin may be had by placing $f_{ZC} < f_{CXO}$.

An additional high-frequency pole is generally added at f_{PWM} to further attenuate ripple and noise at f_{PWM} and higher. This is done by adding a small-value capacitor, C_{pc}, across the $R_{zc}C_{zc}$ network.

$$Cpc = \frac{1}{2\pi \times f_{PWM} \times Rzc} \quad (26)$$

通常在Fpwm增加一个额外的高频极点，来减弱在Fpwm和更高频率的纹波的噪声。这里用一个小电容Cpc并联在RzcCzc网络上实现。

The procedure above is valid for fixed-value inductors. 以上推倒过程对固定电感有效

NOTE

If a "swinging-choke" boost inductor (inductance decreases with increasing current) is used, f_{CXO} varies with inductance, so C_{ZC} should be determined at maximum inductance.

如果使扼流电感（电感随着电流上升而减小），Fcxo随电感量变化，所以Czc必须在最大电感时求出。

Voltage Loop Compensation 电压环补偿

The outer voltage control loop of the dual-phase PFC controller functions the same as with a single-phase controller, and compensation techniques for loop stability are standard [4]. The bandwidth of the voltage-loop must be considerably lower than the twice-line ripple frequency (f_{2LF}) on the output capacitor, to avoid distortion-causing correction to the output voltage. The output of the voltage-error amplifier (VA) is an input to the

双相PFC控制器的外部电压控制环与单相控制器的一样，环路稳定的补偿方式参考【4】。电压环带宽必须要比输出电容上的双线纹波频率要低，以避免对输出电压造成畸变校正。电压误差放大器（VA）的输出是乘法器的一个输入，用来调节输入电流幅度与输出功率。在电流环宽带内VAO上的变化将会影响输入电流的波形。由于在Cout上的低频纹波只是输入功率的函数，那它的峰峰幅值在高压和低压输入时是一样的。任何电压环的响应到这个纹波上会使输入电流变形并且高压输入电流会比低压输入电流变形更大。因此，输入电流三次谐波畸变率可接受范围应该在高压输入情况下确定。

Because the voltage-error amplifier (VA) is a transconductance type of amplifier, the impedance on its input has

因为电压误差放大器（VA）是一个跨导型放大器，所以放大器的增益与它的输入阻抗无关，它只与跨导结果和输出阻抗有关。这样VSENSE的输入分压网络的值可以按VINAC章节的讨论获得。它的输出是VAO引脚

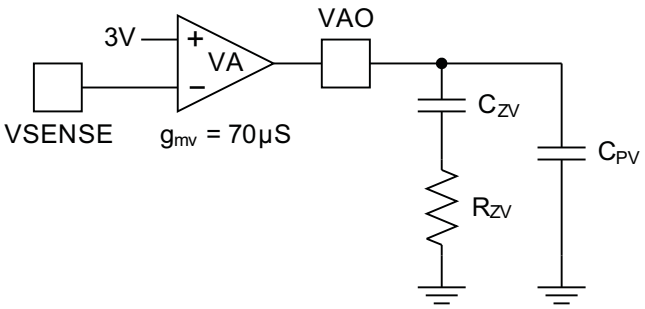


Figure 23. Voltage Error Amplifier With Type II Compensation

The twice-line ripple voltage component of VSENSE must be sufficiently attenuated and phase-shifted at VAO to achieve the desired level of 3rd-harmonic distortion of the input current wave-shape [4]. For every 1% of

VSENSE上的双线纹波电压成分一定要充分减弱，同时VAO相位偏移来获得输入电流波形的三次谐波畸变等级。每1%的三次谐波畸变允许率,在整个VAO电压范围内双线频率上的小信号增益Gvea = VAOpk/VSENSEpk = Gmv*Zov不能超过2%。在UCC28070中，VAO可以在零负载时的1V上升到满载时的4.2V，整个功率范围内有3.2V的变化量，它的2%就是64mV的峰值纹波。

NOTE

Although the maximum VAO voltage is clamped at 5 V, at full load V_{VAO} may vary around an approximate center point of 4.2 V to compensate for the effects of the quantized feed-forward voltage in the multiplier stage (see Multiplier Section for details). Therefore, 4.2 V is the proper voltage to use to represent maximum output power when performing voltage-loop gain calculations.

The output capacitor maximum low-frequency zero-输出电容低频的0到峰值的纹波电压最大值可近似地由下式得出：

$$v_{0\,pk} = \frac{Pin_{avg} \times X_{Cout}}{Vout_{avg}} = \frac{Pin_{avg}}{Vout_{avg} \times 2\pi \times f_{2LF} \times Cout} \tag{27}$$

where $P_{IN(avg)}$ is the total maximum input power 式中Pin(avg)是交错PFC预调节器总的最大输入功率，Vout(avg)是平均输出电压，Cout是输出电容
output voltage and C_{OUT} is the output capacitance.

$V_{SENSEpk} = v_{opk} x k_R$, where k_R is the gain of the resi Kr是在VSENSE上的电阻分压网络增益

Thus, for k_{3rd}% of allowable 3rd-harmonic distortion on the input current attributable to the VAO ripple,

$$Z_{OV(f_{2LF})} = \frac{k_{3rd} \times 64mV \times Vout_{avg} \times 2\pi f_{2LF} \times Cout}{g_{mv} \times k_R \times Pin_{avg}} \tag{28}$$

VAO上的阻抗通过一个电容（Cpv）设置，如下式

This impedance on VAO is set by a capacitor (Cpv), where $C_{PV} = 1/(2\pi f_{2LF} x Z_{OV}(f_{2LF}))$ therefore,

$$Cpv = \frac{g_{mv} \times k_R \times Pin_{avg}}{k_{3rd} \times 64mV \times Vout_{avg} \times (2\pi f_{2LF})^2 \times Cout} \tag{29}$$

The voltage-loop unity-gain cross-over frequency (f_{VXO}) may now be solved by setting the open-loop gain equal to 1:

电压环单位增益交越频率Fvxo可按下式计算得到

$$Tv(f_{VXO}) = G_{BST} \times G_{VEA} \times k_R = \left(\frac{Pin_{avg} \times X_{Cout}}{\Delta V_{VAO} \times Vout_{avg}}\right) \times \left(g_{mv} \times X_{Cpv}\right) \times k_R = 1 \tag{30}$$

$$f_{VXO}{}^2 = \frac{g_{mv} \times k_R \times Pin_{avg}}{\Delta V_{VAO} \times Vout_{avg} \times (2\pi)^2 \times Cpv \times Cout}$$

so, (31)

The “zero-resistor” (R_{ZV}) from the zero-placement network of the compensation may now be calculated. Together with C_{PV}, R_{ZV} sets a pole right at f_{VXO} to obtain 45° phase margin at the cross-over.

$$Rzv = \frac{1}{2\pi f_{VXO} \times Cpv}$$

Thus, (32)

Finally, a zero is placed at or below $f_{VXO}/6$ with capacitor C_{ZV} to provide high gain at dc but with a breakpoint far enough below f_{VXO} so as not to significantly reduce the phase margin. Choosing $f_{VXO}/10$ allows one to approximate the parallel combination value of C_{ZV} and C_{PV} as C_{ZV}, and solve for C_{ZV} simply as:

$$Czv = \frac{10}{2\pi f_{VXO} \times Rzv} \approx 10 \times Cpv \tag{33}$$

By using a spreadsheet or math program, C_{ZV}, R_{ZV}, and C_{PV} may be manipulated to observe their effects on f_{VXO} and phase margin and %-contribution to 3rd-harmonic distortion (see note below). Also, phase margin may be checked as $P_{IN(avg)}$ level and system parameter tolerances vary.

NOTE

The percent of 3rd-harmonic distortion calculated in this section represents the contribution from the f_{2LF} voltage ripple on C_{OUT} only. Other sources of distortion, such as the current-sense transformer, the current synthesizer stage, even distorted V_{IN}, etc., can contribute additional 3rd and higher harmonic distortion.

Advanced Design Techniques 先进的设计技术

Current Loop Feedback Configuration 电流环反馈结构 (Sizing of the Current Transformer Turns Ratio and Sense Resistor (R_S) 电流互感器和检测电阻大小

A current-sense transformer (CT) is typically used in high-power applications to sense inductor current while avoiding significant losses in the sensing resistor. For average current-mode control, the entire inductor current

电流互感器常用于大功率应用上用来检测电感电流，避免使用检流电阻产生太多的损耗。对于平均电流模式控制，全部的电感电流波形是必要的；然而低频互感器明显不能满足要求。通常需要使用两个高频互感器，一个在开关臂用来获得上升斜坡电流，另一个在二极管臂用来获得下降斜坡电流。这两个电流信号合到一起得到完整的电感电流，但这不是UCC28070的菜。

A major advantage of the UCC28070 design is the current synthesis function, which internally recreates the

UCC28070的一个突出的优势就是电流合成功能，它能在芯片内重现开关周期中关断时间内电感电流的下降斜坡。这样在二极管臂的电流互感器就不需要了，减小了体积节省了成本。按电流合成器章节所述，用一个信号电阻就能设置好合成器的下降斜坡。

slope, as previously discussed in the Current Synthesizer section.

A number of trade-offs must be made in the selection of the CT. Various internal and external factors influence the size, cost, performance, and distortion contribution of the CT.

电流互感器的选择要做一些权衡。各种内部外部的因素会影响到互感器的大小，成本，性能和失真度

- Turns-ratio (N_{CT}) 匝比
- Magnetizing inductance (L_M) 磁化电感
- Leakage inductance (L_{LK}) 漏感
- Volt-microsecond product (Vμs) V-us
- Distributed capacitance (C_d) 分布电容
- Series resistance (R_{SER}) 串联电阻
- External diode drop (V_D) 外部二极管压降
- External current sense resistor (R_S) 外部检流电阻
- External reset network 外部重置网络

Traditionally, the turns-ratio and the current sense resistor are selected first. Some iterations may be needed to refine the selection once the other considerations are included.

通常，先确定匝比和检流电阻大小。加上其它条件后还需要一些重复计算来完善结果。

In general, 50 < N_{CT} < 200 is a reasonable range from which to choose. If N_{CT} is too low, there may be high

一般来说，Nct的合理取值在50-200之间。如果Nct太小，在Rst Lm上的损耗就会很大。而如果Nct太大，Lk和Cd上的损耗就会很大。（假定初级线圈是1匝）

winding is assumed.)

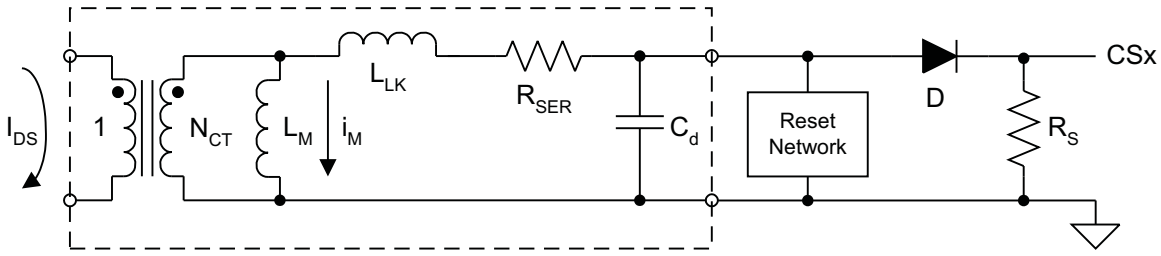


Figure 24. Current Sense Transformer Equivalent Circuit

A major contributor to distortion of the input current is the effect of magnetizing current on the CT output signal (i_{RS}). A higher turns-ratio results in a higher L_M for a given core size. L_M should be high enough that the magnetizing current (i_M) generated is a very small percentage of the total transformed current. This is an impossible criterion to maintain over the entire current range, because i_M unavoidably becomes a larger fraction

主要的输入电流畸变是CT输出信号上磁化电流造成的。对于一个给定的磁芯，高匝比导致的结果是高Lm。Lm要足够大，这样磁化电流Im才能产生一个很小的总互感电流百分比。这在整个电流范围内是不可能的，因为在输入电流减小到零时Im不可避免的占了Irs很大的一部分。导致Im会从Rs上“偷走”一部分信号电流，减小了CSx电压和实际检测到的电流。在低电流时，这将尤为明显，同时CAOx会增加电流环占空比试图校正CSx输入和IMO基准电压的匹配。这种不必要的校正导致在输入波形上CT处的过大的电流，像在AC线路靠近过零处。在高压输入代负载输出时它可能在一定程度上影响到整个波形。

The sense resistor R_S is chosen, in conjunction with N_{CT}, to establish the sense voltage at CSx to be about 3 V at the center of the reflected inductor ripple current under maximum load. The goal is to maximize the average signal within the common-mode input range V_{CMCAO} of the CAOx current-error amplifiers, while leaving room for

检流电阻Rs的选择，要联合Nct，在整流后的电感纹波电流中心值、最大负载下，使检测电压约为3V。目的是最大程度的减小CAOx电流放大器的共模输入范围Vcmcao的平均信号，为Vcmcao纹波电流峰值留下空间。设计条件必须在乘法器章节中最低的电大输入功率限制处。如果电感纹波电流太高导致Vcsx超过Vcmcao，那么Rs或Nct或两个都要作调整来减小Vcsx，这就能减小平均检测电压中心低于3V。这种情况下没什么错，但要注意与轻载时潜在的畸变相比，这个信号在满载和空载之间被压缩得更多。

The matter of volt-second balancing is important, especially with the widely varying duty-cycles in the PFC stage. Ideally, the CT is reset once each switching period; that is, the off-time Vμs product equals the on-time Vμs product. (Because a switching period is usually measured in microseconds, it is convenient to convert the volt-second product to volt-microseconds to avoid sub-decimal numbers.) On-time Vμs is the time-integral of the voltage across L_M generated by the series elements R_{SER}, L_{LK}, D, and R_S. Off-time Vμs is the time-integral of the voltage across the reset network during the off-time. With passive reset, Vμs-off is unlikely to exceed Vμs-on. Sustained unbalance in the on or off Vμs products will lead to core saturation and a total loss of the current-sense signal. Loss of V_{CSx} causes V_{CAOx} to quickly rise to its maximum, programming a maximum duty-cycle at any line condition. This, in turn causes the boost inductor current to increase without control, until the system fuse or some component failure interrupts the input current.

伏秒平衡也很重要，特别是在PFC上有很大的占空比变化。理想状况下，互感器在每个周期重置一次，也就是关断时间的Vus等于导通时间的Vus（因为开关周期通常在微秒级，为了计算方便就将伏-秒转换成伏-微秒）。导通时间的Vus是由串联元件Rser,Llk,D,和Rs产生的穿过Lm的电压在时间上的积分。关断时间的Vus是穿过重置网络的电压的时间积分。使用被动复位，Vus-off不可能大过Vus-on。长时间的伏秒不平衡将会导致磁芯饱和，和电流检测信号损耗。Vcsx的损耗导致Vcaox很快上升到它的最大值，在任何输入情况下都是最大占空比的设置。这将使升压电感电流不受控的上升，直到系统保险丝烧断或别的元件失效才中断输入电流。

It is vital that the CT has plenty of Vμs design-margin to accommodate various special situations where there to

至关重要的是，电流互感器要用冗余设计，来容纳在一些最大输入电流输入的情况下的连续在大占空比周期，如在峰值电流限制点时。

Maximum Vμs(on) can be estimated by:

最大的Vus(on)可按下式得

$$V_{\mu(on)max} = t_{ON(max)} \times \left(V_{RS} + V_D + V_{RSER} + V_{LK}\right) \quad (34)$$

where all factors are maximized to account for worst-case transient conditions and $t_{ON(max)}$ occurs during the lowest dither frequency when frequency dithering is enabled. For design margin, a CT rating of ~5*Vμs(on)max or higher is suggested. The contribution of V_{RS} varies directly with the line current. However, V_D may have a significant voltage even at near-zero current, so substantial Vus(on) may accrue at the zero-crossings where the

式中所有因子都按最大取值来作为最坏情况，若使用了频率振荡Ton(max)要在最小频率时取。为了设计裕度，建议CT额定为5*Vus(on)max或更大。Vrs直接与线路电流成正比。然而，甚至在零电流附近Vd可能还有一个电压，所以在占空比最大时过零处Vus(on)可能有积累。Vrser的影响最小，通常在Rser<<Rs时可以忽略。Vlk由检测电流的di/dt决定，并不能在外部被观察。然而，鉴于电流信号的亚微秒上升时间加电感电流斜坡，它的影响非常大。幸运的是，大部分在导通时间内形成的Vus在占空周期下降沿的下降时间内被消除，还有小部分在关断时间内被重置。虽然如此，CT还是必须至少要能在一个开关周期里关断之前完全建立好内部Vus(on)max。

Vμs(off) may be generated with a resistor or zener diode, using the i_M as bias current.

Vus(off)可由下面的电路得

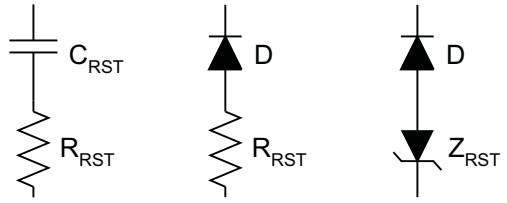


Figure 25. Possible Reset Networks

In order to accommodate various CT circuit designs and prevent the potentially destructive result due to CT saturation, the UCC28070's maximum duty-cycle needs to be programmed such that the resulting minimum off-time accomplishes the required worst-case reset. (See the PWM Frequency and Duty-Cycle Clamp section of the data sheet for more information on sizing R_{nct}.) Be aware that excessive C_d in the CT can interfere with be made.

为了调整不同CT电路设计并避免可能存在的有害结果导致CT饱和，UCC28070的最大占空比需要被控制这样最小关断时间实现最坏情况重置。要注意CT上极端的Cd会有碍于高效的重置，因为直到CT自谐振频率的1/4周期之后重置电压都还没达到最大值。匝比越大Cd就越大，所以在Nct和Dmax之间要权衡利弊。

The selected turns-ratio also affects L_M and L_{LK}, which vary proportionally to the square of the turns. Higher L_M is (

匝比也会对Lm和Llk有影响，两者与匝数的平方成正比。Lm越大越好，而Llk要越小越好。假设在导通时间内Lm两端电压不变，那磁化电流是一个上升的斜坡。

This upward ramping current subtracts from i_{RS}, which affects V_{CSx} especially heavily at the zero-crossings and light loads, as stated earlier. With a reduced peak at V_{CSx}, the current synthesizer starts the down-slope at a lower voltage, further reducing the average signal to CAOx and further increasing the distortion under these conditions. If low input current distortion at very light loads is required, special mitigation methods may need to be developed to accomplish that goal.

这个上升斜坡从Irs中减掉，它在过零处和轻载时对Vcsx的影响特别严重。在Vcsx上峰值的减小，电流合成器在较低电压时开始下降斜坡，随之而来的就是CAOx平均信号的减小和在这些情况下的畸变的增加。如果要求在很轻的负载时有很小的输入电流变形，可能需要为之设计特殊的减缓方法。

Current Sense Offset and PWM Ramp for Improved Noise 电流检测偏置和增强抗干扰性能的PWM斜坡

To improve noise immunity at extremely light loads, a PWM ramp with a dc offset is recommended to be added to the current sense signals. Electrical components R... R... R... R... C... C... D... D... D... D... C...

为了提高外部轻载时的抗干扰性，推荐给电流检测信号加上一个带直流偏置的PWM斜坡。
Rta,Rtb,Roa,Cta,Ctb,Dpa1,Dpb1,Dpa2,Dpb2,Cta,Ctb构成PWM斜坡，它由UCC28070的门极驱动输出带动工作。

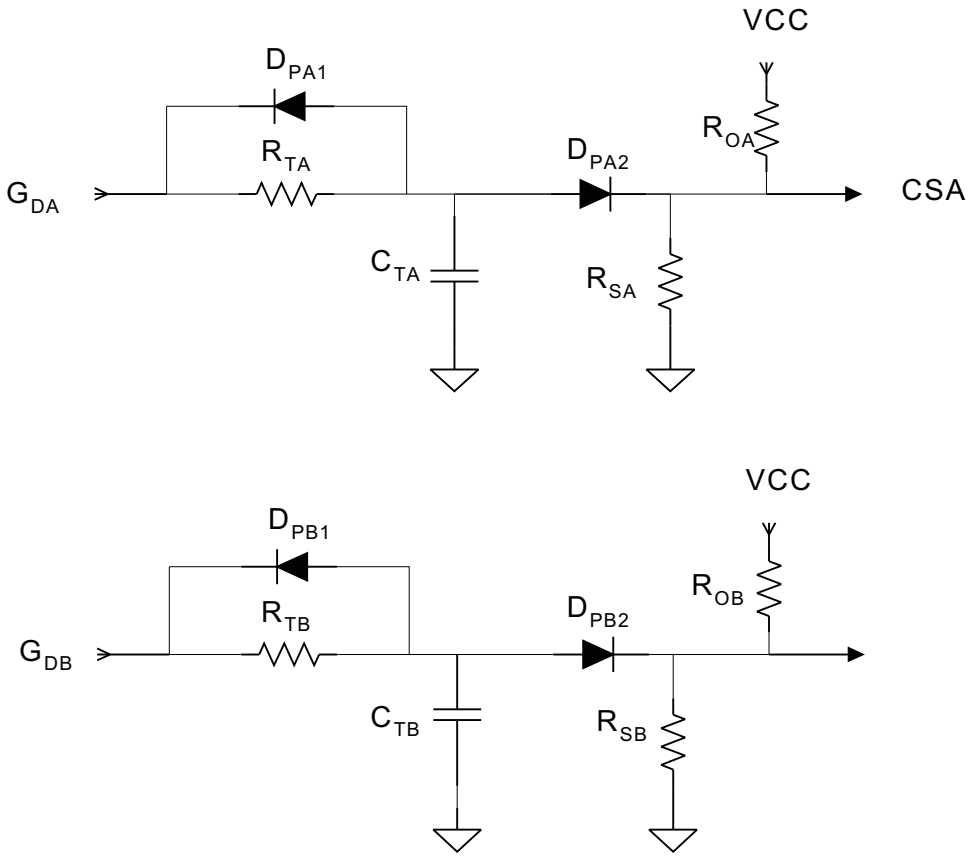


Figure 26. PWM Ramp and Offset Circuit

When the inductor current becomes discontinuous the boost inductors ring with the parasitic capacitances in the boost stages. This inductor current rings through the CTs causing a false current sense signal. Please refer to
在升压阶段，当电感电流不连续时升压电感与其等效电容发生振荡。这个振荡经过CTs后会造成错误的电流检测信号。电感电流不连续时检测电流信号可参考下面的图。

NOTE

The inductor current and RS may vary from this graphical representation depending on how much inductor ringing is in the design when the unit goes discontinuous.

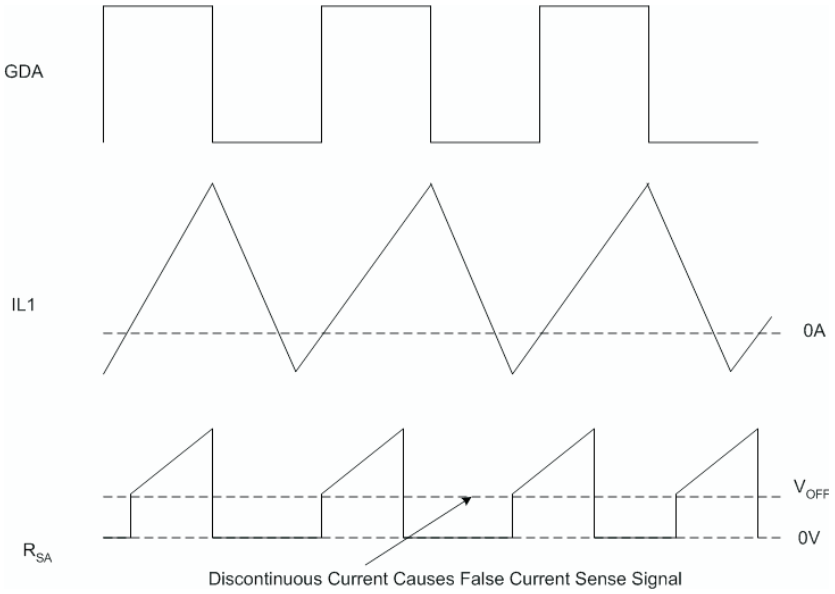


Figure 27. False Current Sense Signal

To counter for the offset (V_{OFF}) just requires adjusting resistors R_{OA} and R_{OB} to ensure that when the unit goes
偏置电压只需要校正电阻Roa和Rob就能确保在不连续时电流应该为零时检测信号得到一个负电流。将偏置电流设置为120mV是个比较好的起始点，然后可能需要根据特殊情况有所调整。

$$R_{SA} = R_{SB} \tag{35}$$

$$R_{OA} = R_{OB} = \frac{(V_{VCC} - V_{OFF})R_{SA}}{V_{OFF}} \tag{36}$$

选择好适当的Rta,Rtb,Cta和Ctb之后就能加上一个等于最大电流检测信号的10%的小PWM斜坡了。

A small PWM ramp that is equal to 10% of the maximum current sense signal (V_S) less the offset can then be added by properly selecting R_{TA}, R_{TB}, C_{TA} and C_{TB}.

$$R_{TA} = R_{TB} = \frac{(V_{VCC} - (V_S \times 0.1 - V_{OFF}) + V_{DA2})R_{SA}}{V_S \times 0.1 - V_{OFF}} \tag{37}$$

$$C_{TA} = C_{TB} = \frac{1}{R_{TA} \times f_S \times 3} \tag{38}$$

Recommended PCB Device Layout PCB布局布线建议

Interleaved PFC techniques dramatically reduce input and output ripple current caused by the PFC boost inductor, which allows the circuit to use smaller and less expensive filters. To maximize the benefits of interleaving, the output filter capacitor should be located after the two phases allowing the current of each phase

交错PFC技术通过PFC升压电感显著减小了输入输出纹波电流，这让电路能使用更小更便宜的滤波器。为了将交错技术的好处最大化，输出滤波电容必须紧跟在两相之后，使每相的电流在进入升压电容前被加在一起。类似于其它的电源管理芯片，PCB布线时使用星状接地技术很重要，它使滤波器和高频旁路电容能尽可能近地和芯片引脚和地连接。为了最小化由升压电感磁耦合可能产生的干扰，芯片必须与升压电感保持至少1inch以上的距离。同样不建议将芯片放置在磁性元件下面。

References

1. O'Loughlin, Michael, "*An Interleaving PFC Pre-Regulator for High-Power Converters*", Texas Instruments, Inc. 2006 Unitrode Power Supply Seminar, Topic 5
2. Erickson, Robert W., "*Fundamentals of Power Electronics*", 1st ed., pp. 604-608 Norwell, MA: Kluwer Academic Publishers, 1997
3. Creel, Kirby *"Measuring Transformer Distributed Capacitance"*, White Paper, Datatronic Distribution, Inc. website: http://www.datatronics.com/pdf/distributed_capacitance_paper.pdf
4. L. H. Dixon, *"Optimizing the Design of a High Power Factor Switching Preregulator"*, Unitrode Power Supply Design Seminar Manual SEM700, 1990. Texas Instruments Literature Number SLUP093
5. L. H. Dixon, *"High Power Factor Preregulator for Off-Line Power Supplies"*, Unitrode Power Supply Design Seminar Manual SEM600, 1988. Texas Instruments Literature Number SLUP087

REVISION HISTORY

Changes from Revision C (June 2009) to Revision D **Page**

- Changed 30 kHz to 300 kHz 1

Changes from Revision D (June 2010) to Revision E **Page**

- Changed PWM switching frequency 4
- Changed Figure 8 12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
UCC28070DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC28070	Samples
UCC28070DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC28070	Samples
UCC28070PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	28070	Samples
UCC28070PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	28070	Samples
UCC28070PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	28070	Samples
UCC28070PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	28070	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF UCC28070 :

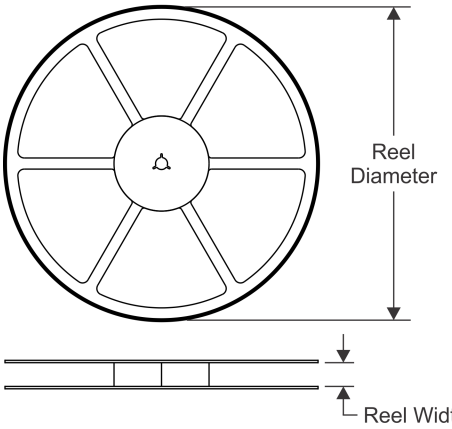
- Automotive: UCC28070-Q1

NOTE: Qualified Version Definitions:

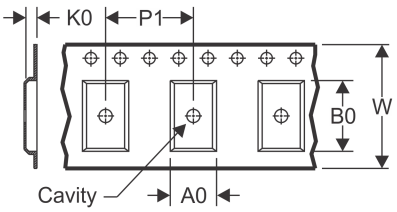
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

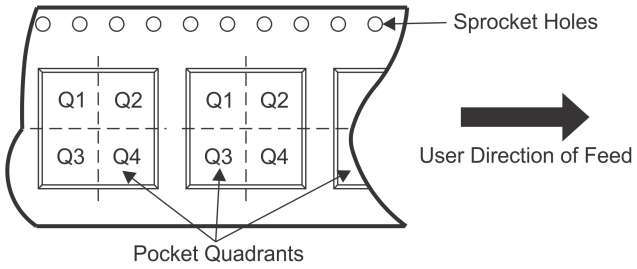


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

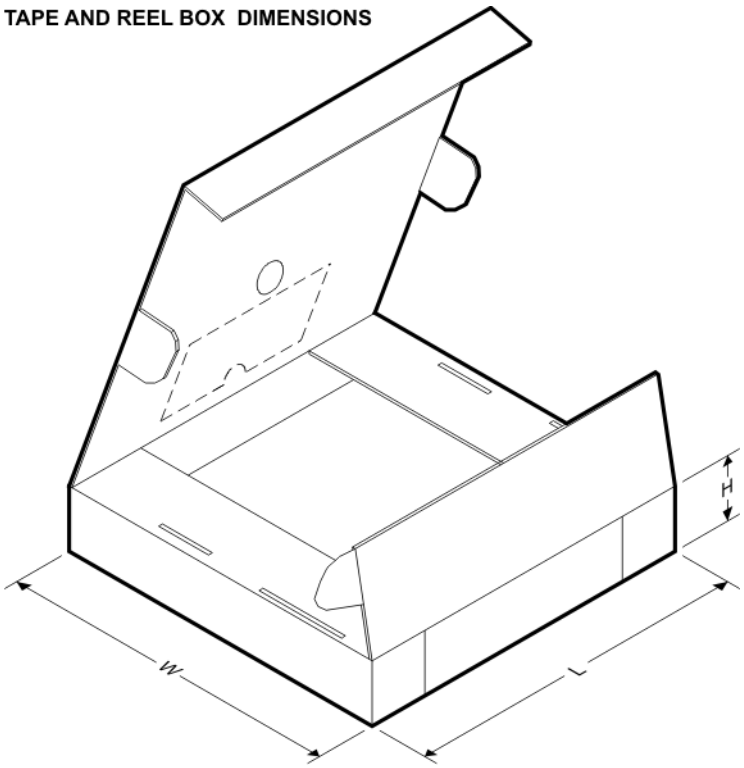
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28070PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

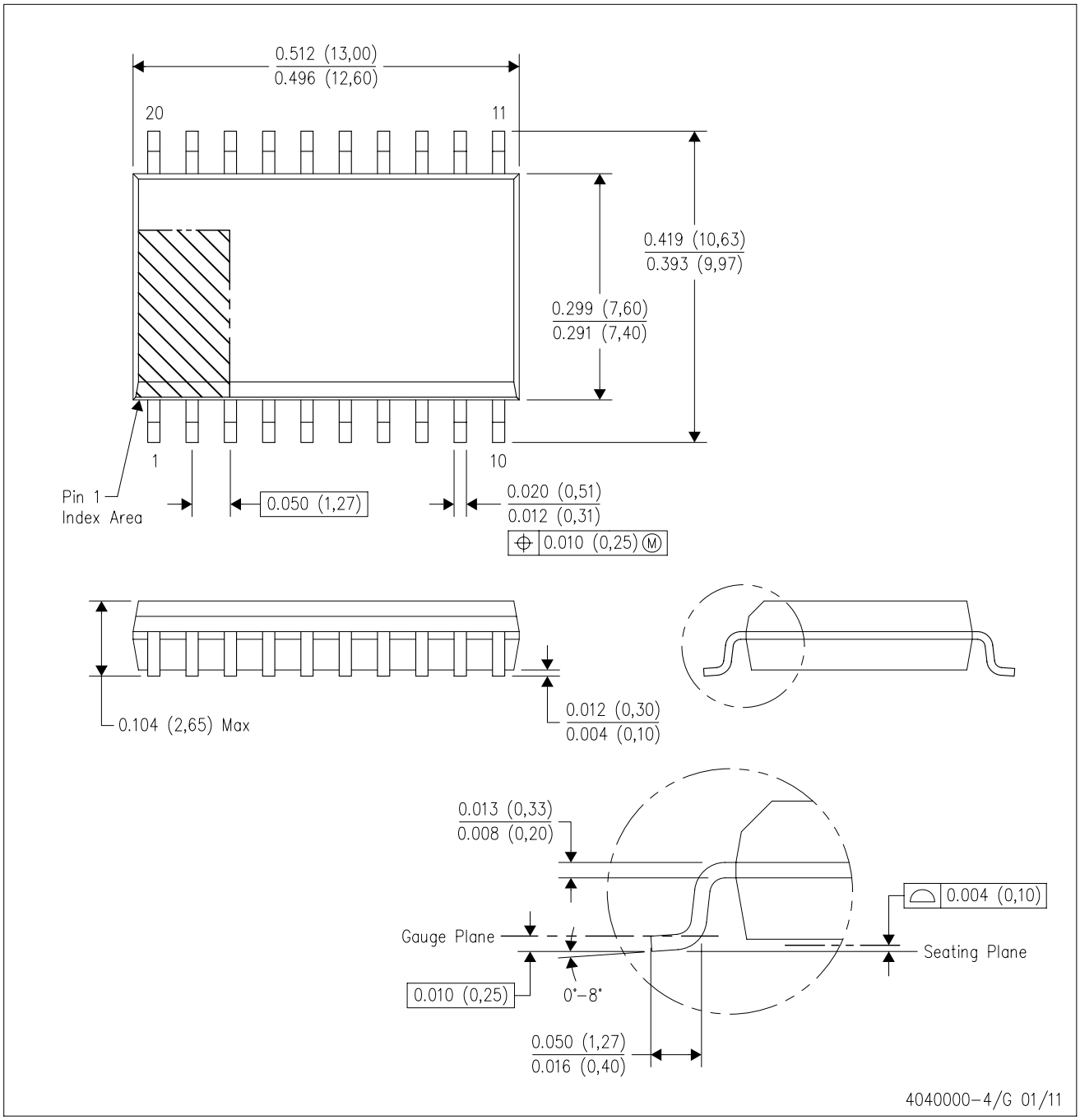
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

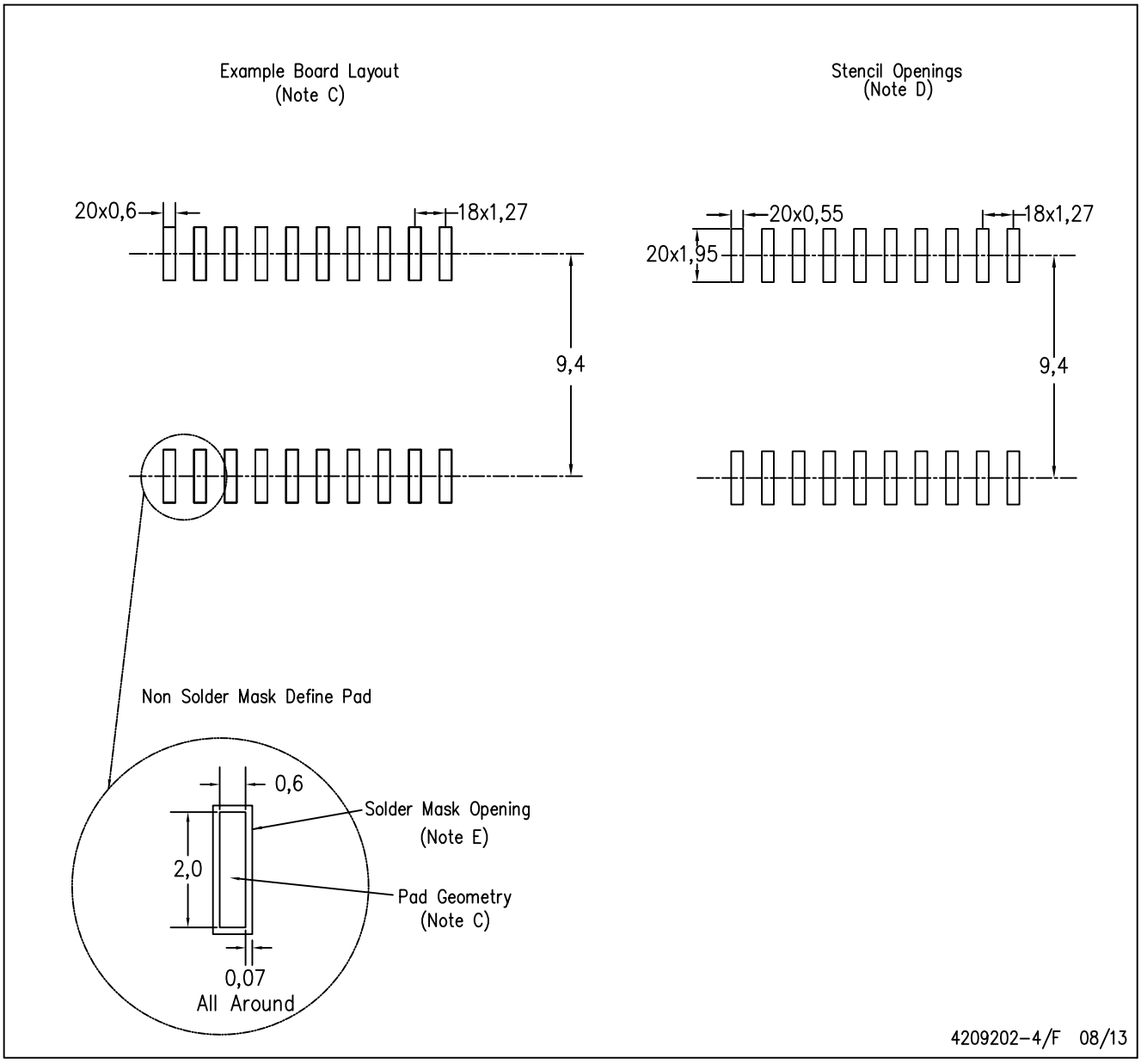
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28070PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



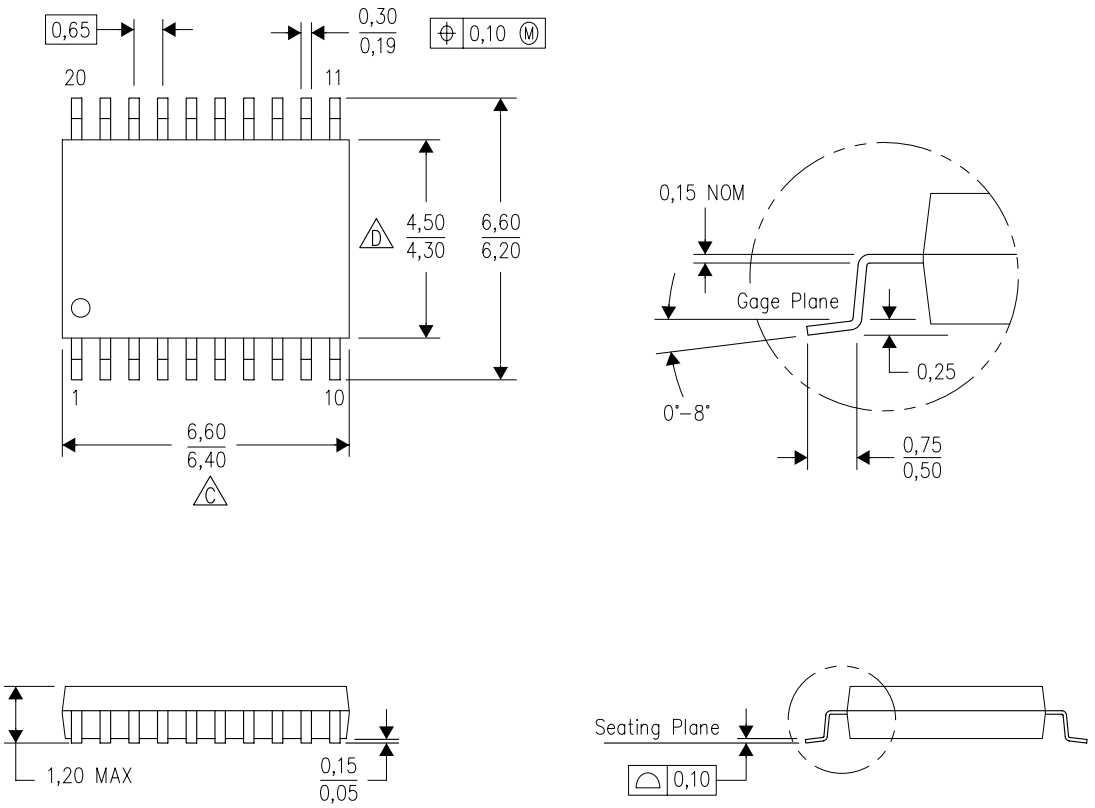
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



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NOTES:
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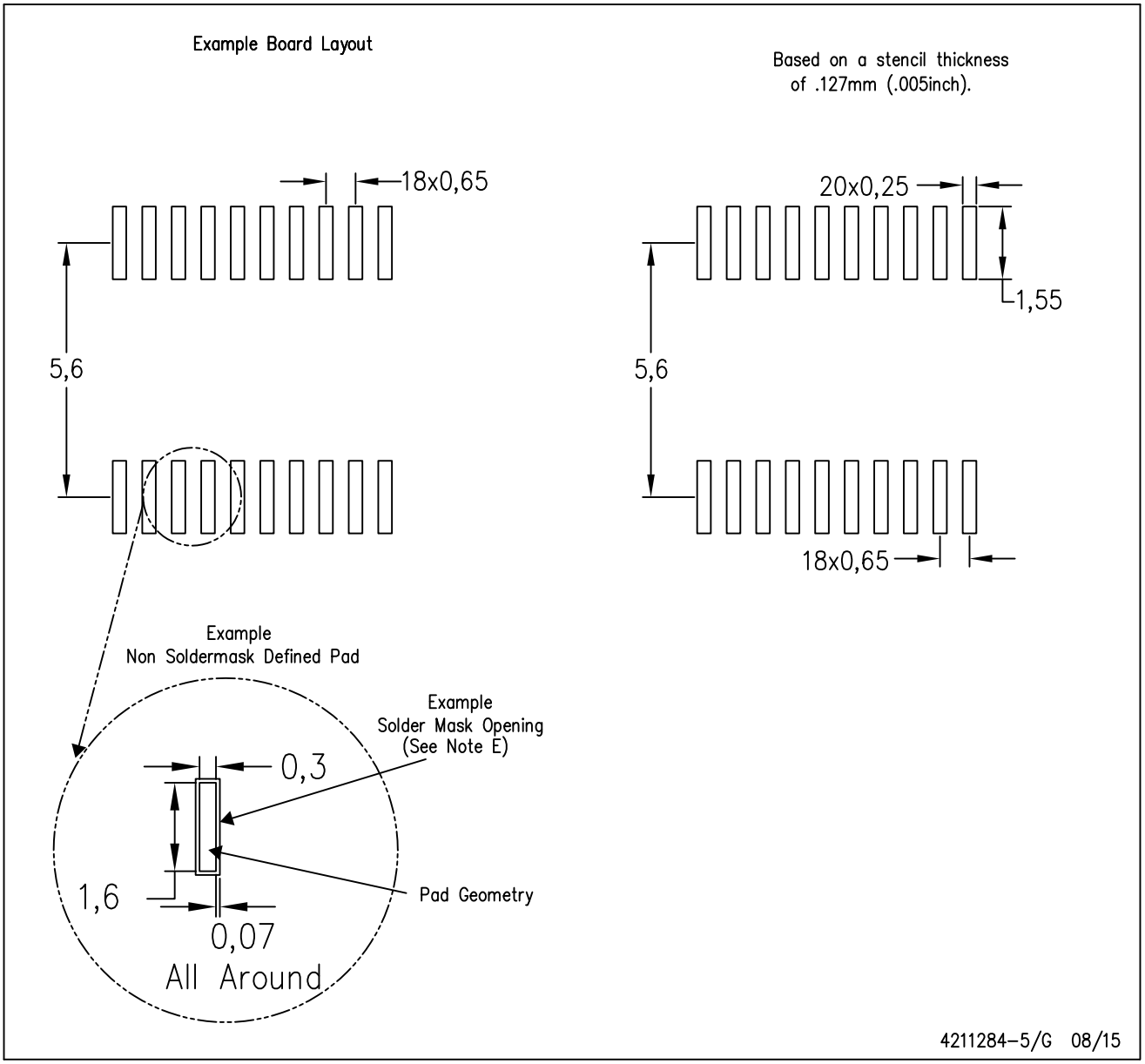
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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